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A Review on Low Power VLSI Design Techniques

R. Arunn Veeraraghavan

Student, Department of Electronics and Communication Engineering, SRM Easwari Engineering College, Chennai, Tamil Nadu, India

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Abstract : *There has been an increase in the electronic gadgets which are being powered by battery. The CMOS circuits play a pivotal role in the development, and due to the reduction in the size of the chip and there is also reduction in power consumption and it has to be optimized and designed accordingly. This paper discusses about the different power dissipation and optimization techniques and helps the designers in the finding the right balance between optimization and performance.*

Key words: **Power dissipation, Static power dissipation, Dynamic power dissipation, Transistor stacking, clock gating.**

1. INTRODUCTION

In the past few decades, there has been an increase in the production and requirement of silicon chips which are used in plethora of industries, ranging from healthcare to computing. The VLSI industry is mainly divided into two categories, BJT based and MOSFET based and the size of the chip has shrunk from, 90nm to 7nm in the recent times. Earlier, majority of designers used to focus more areas such as performance, design and cost but, in the recent times the designers placed a greater emphasis on the power consumption, dissipation and also in usage of low power consuming components. The main aim or goal for the chip designers is to extract maximum performance with minimum power as the chips have shrunk in size. So, with less power dissipation, we generate less heat and which in turn reduces the cost of packaging and cooling techniques and with the increase in the amount of battery powered devices (For e.g.:- Smartphones, laptops, etc.) the developers are more focused on the power consumption. This paper mainly focuses on various causes and types of power dissipation, low power design techniques and the power management strategies.

2. TYPES OF POWER DISSIPATION

There are different ways by which power dissipation occurs and they are broadly classified into two types:-

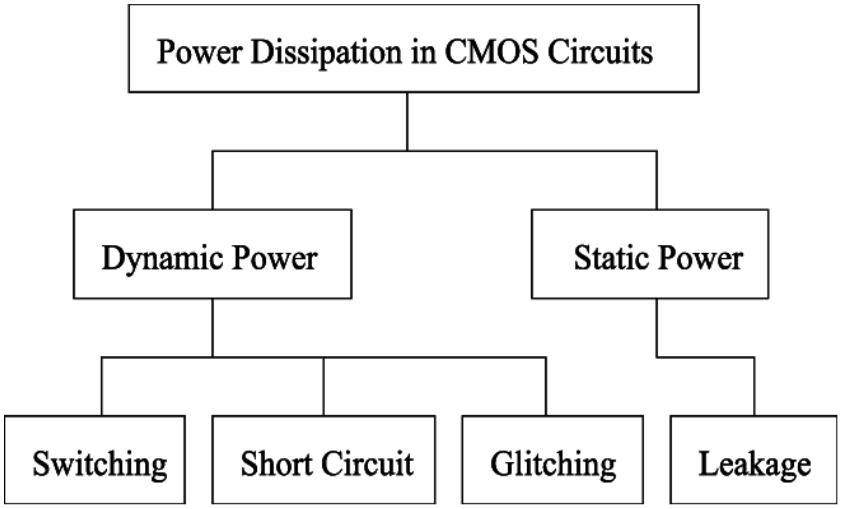

Figure 1: Power Dissipation Flowchart

1. Static power dissipation

2. Dynamic power dissipation

The total power dissipated in any circuit is given by the term

$$P_{Total} = P_{Dynamic} + P_{Static} + P_{Short\ circuit}$$

The main difference between the static and dynamic power dissipation, is the former occurs when the circuit is idle and the latter occurs when the circuit is actively switching from one state to another. It may also consume power while the charging and discharging operations.

2.1 DYNAMIC POWER DISSIPATION

$$P_{Total} = \alpha\, f*C*V_{dd}^2 + f* I_{short}* V_{dd} + I_{leak}* V_{dd}$$

Where,

α = Switching factor, C = Load capacitance

V_{dd} = Voltage

f = Clock frequency

I_{Short} = Short circuit current

I_{leak} = Leakage current

The dynamic power loss is further divided into two more types: short circuit, switched power dissipation and it depends on the factors like voltage, capacitance, and frequency. The use of lower value of V_{dd} helps in reducing the power dissipated but it leads to degradation in performance.

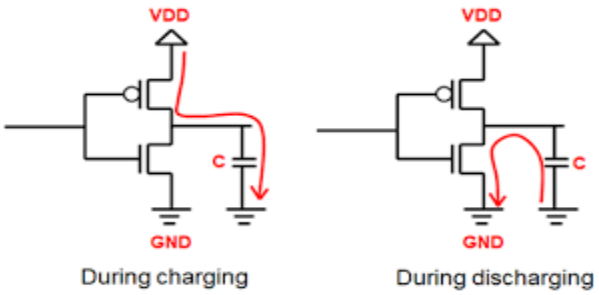

Figure 2: Dynamic power Dissipation

2.2 SWITCHING POWER DISSIPATION

In CMOS circuits, there are large number of capacitors and parasitic, gate capacitance is present. There are two networks namely Pull up network, made of pMOS transistors and Pull down network made of nMOS transistors, the capacitors gets charged and discharged during various operations and the charging happens through the P-type devices in Pull up network, the discharging occurs through the Pull down network.

2.3 SHORT CIRCUIT POWER DISSIPATION

In, short circuit power dissipation when the input voltage (V_{dd}) is higher than that of the threshold voltage, the NMOS is said to be in ON state and the pMOS in the OFF state. If the input voltage is less than the threshold voltage ($V_{dd} - V_{tn}$)

in pMOS, the vice-versa happens. For a short interval of time, when the input hovers between the values of V_{dd} and (V_{dd}-V_{tn}) both the nMOS and pMOS are in the ON state.

The Short circuit power dissipation is represented by the term:

$$P_{\text{Short circuit}} = \beta/12 * (V_{dd} - 2V_{th})^3 * \tau/T_p$$

2.4 GLITCHING

The glitching power dissipation, occurs due to both switching and short circuit dissipation and is considered the main reason for the phenomenon. The glitch usually occurs at the output, and it largely depends on the gates used, logic and function. The glitches lead to short circuit power dissipation when, there is a transiton of state occurs and the voltage is at an alarmingly high values and can be negated by changing the input and threshold voltage.

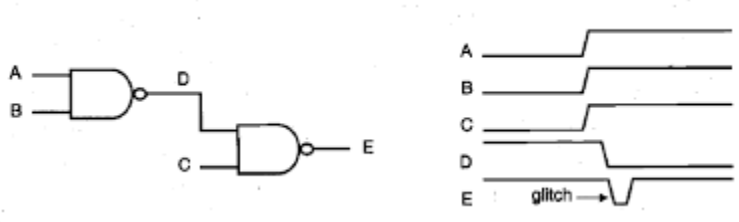

Figure 3: Output showing glitch

2.5 STATIC POWER DISSIPATION

The static power dissipation occurs when the circuit is idle, and is called as leakage power and it occurs when the voltage is scaled up, and the transistor enters the sub-threshold state, which leads to reverse current (i.e. current flowing from oxide to P-N) and causes leakage power. This phenomenon, can be controlled by multiple threshold voltage, body bias and transistor stacking.

3. POWER MANAGEMENT TECHNIQUES

There are various techniques by which power management can be implemented in a CMOS circuit by making some corrections in the design:-

3.1 STATIC POWER OPTIMIZATION

1. Multiple threshold voltage (V_{th})

   This technique is used to reduce the leakage and standby power dissipation in CMOS circuits, by using various levels of threshold voltage for different state in which the circuit is being used. So, for minimizing leakage current, there should be high threshold voltage and when the device is in operation mode, the threshold voltage is set low to get high performance. The glitches in a circuit can be eliminated using this technique.

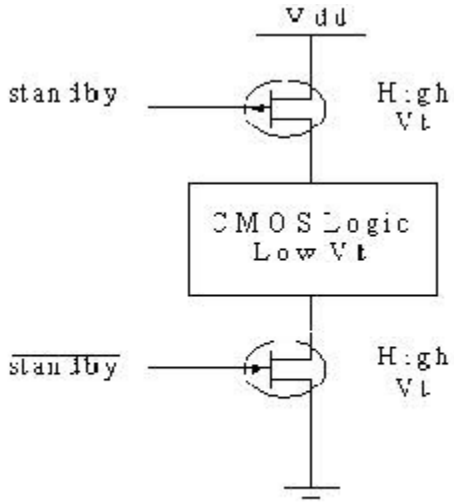

Figure 4: CMOS circuit (Multi threshold voltage)

2. Body biasing technique

   It's a technique by which we connect transistors to a bias, rather than connecting it to the source voltage or the ground. This is done to produce a strong inversion at the channel and we don't want the drain current to be leaked while transmitting and to get low leakage currents, reverse body biasing is done between drain and body.

3. Transistor stacking

   In this technique, two transistors which are in off state are connected together in series cause significantly less leakage of power when compared to a one transistor in off position. It depends on source voltage, so with increase in the source voltage there is a decrease in the sub threshold current.

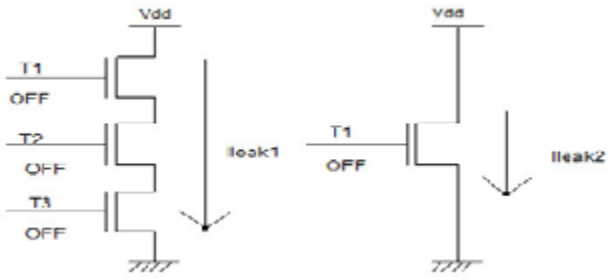

Figure 5: Transistor stacking

4. Lector approach

   The LECTOR technique is used to handle the leakage current, without increasing the dynamic power dissipation in CMOS circuits. There are two transistors included in the circuit, namely leakage control transistor and the source of one transistor controls the gate of the other transistor thereby increasing resistance from the ground and decreasing leakage. This method works in both active and non-active state of the transistor.

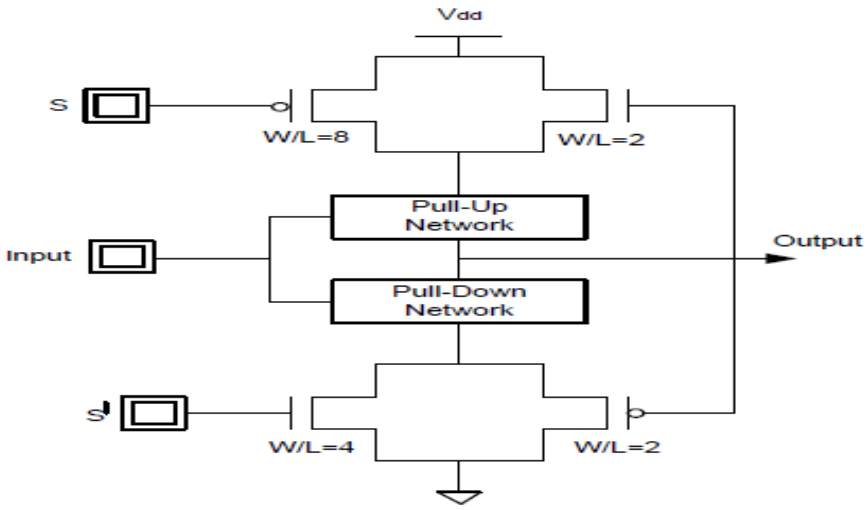

Figure 6: Lector Technique

3.2 DYNAMIC POWER OPTIMIZATION

1. Multiple source voltage (V_{dd})

   The advantage of having multiple source voltage is that, it is useful in eliminating both static and dynamic power dissipation. There are different supply voltages for different modes, the high performance modes get high V_{dd} and the low performance mode is assigned with low supply voltage. Thus it is used for deriving high performance and also to reduce power dissipation.

2. Dynamic voltage and frequency scaling

   The circuits require different power for handling different types of activities, so on decreasing the clock frequency there is a decrease in the source voltage and can be used to save power, the main advantage of this technique is that the processing speed and performance improves. The processor or the device decides the frequency for the task and sets a threshold with room for improvement in the frequency required.

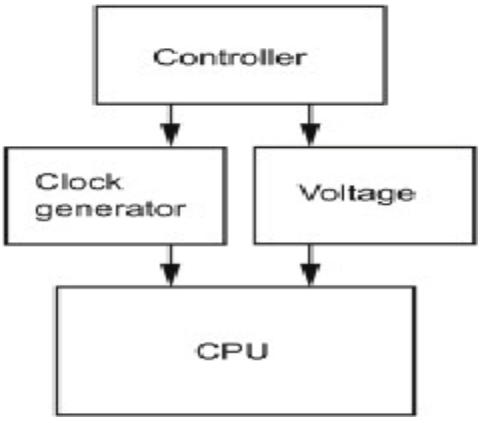

Figure 7: Dynamic voltage and frequency scaling

3. Clock gating

The clock gating is an approach by which, the power dissipation in the circuit can be controlled by reducing the frequency of blocks, which is being activated less or disabling them. This technique also helps out reducing the unwanted switching activities and thereby helps out in power saving. The clock gating is done at the architecture level.

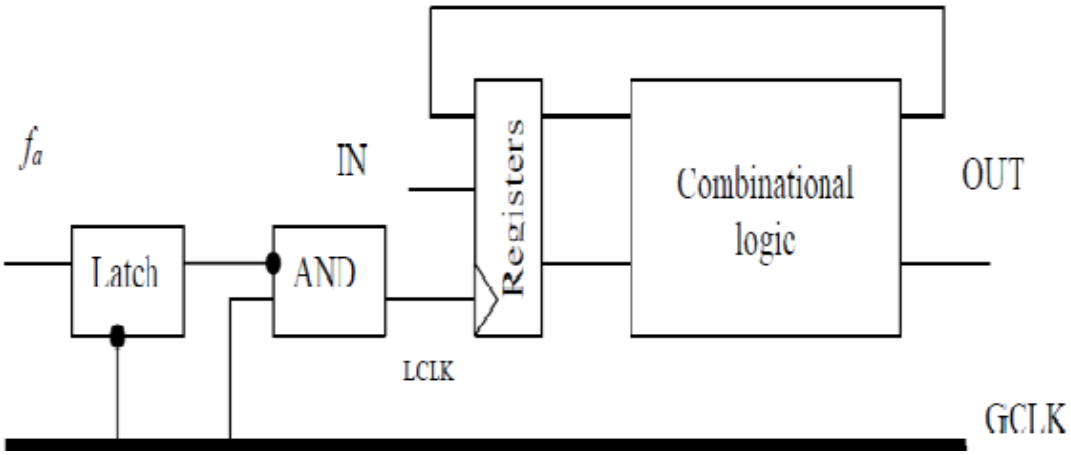

Figure 8: Clock gating

4. CONCLUSION

This paper discusses about the power dissipation and the ways by which low power circuits can be designed at logic and architectural level have been discussed. Power dissipation is one of the major challenges designers are finding difficult to deal with and there has been constant evolution. The paper helps the reader understand the basics of power dissipation and how it is being dealt with in the industry.

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