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SIMULATION OF HYBRID HVDC CIRCUIT BREAKER WITH SFCL FOR FAULT CURRENT LIMITING

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Abstract - *Recently, studies on HVDC circuit breaker (CB) prototypes have become popular among power system researchers. In this paper, a novel hybrid-type superconducting DCCB model (SDCCB) is proposed. The SDCCB has a superconducting fault current limiter (SFCL) located in the main line, to limit the fault current. After the trip signal, Electronic (IGBT) switches located in the main line will commutate the fault current into a parallel line, where dc current is forced to zero by combination of IGBTs and surge arresters. To check performance of the SDCCB, a simulation analysis for SDCCB current interruption performance is done in MATLAB software for three different systems which are denoted as "Normal System," "Strong System," and "Very Strong System". The current limiting by the SFCL notably suppressed the dc fault current and significantly reduced the current interruption stress for SDCCB components.*

Key Words: **D.C circuit breaker (DCCB), High-voltage direct current (HVDC), Hybrid DCCB (HDCCB), Multi terminal HVDC, Superconducting fault current limiter (SFCL), Voltage source converters (VSC).**

1. INTRODUCTION

High voltage direct current (HVDC) technology is a key component in the future energy system based on renewable energy sources, such as wind and solar power which are often both volatile and remotely located and with the development of power electronics technology, HVDC system has attracted widespread attention of researchers. HVDC transmission line costs is less than an AC line and have a lower environmental impact because they require fewer overhead lines to deliver the same amount of power as HVAC systems. However, it is also true that HVDC terminal stations are more expensive due to the fact that they must perform the conversion from AC to DC, and DC to AC. But over a certain distance, the so called "break-even distance" (approx. 600 – 800 km), the HVDC alternative will always provide the lowest cost compared to HVAC system.

Voltage Source Converter-High Voltage Direct Current (VSC-HVDC) is the most efficient and reliable method for electrical power transmission over long distances. The greatest challenge with VSC-HVDC system is very high short-circuit faults current which may damages the converter valves and the transmission network. Conventional DC breakers are not fast enough and reliable to provide adequate protection for DC faults on multi-terminal networks. Hence, good technology based HVDCCB is required to isolate faults. For fast fault elimination it is required to absorb fault current quickly. Some of the methods adopted for absorption and dissipation of energy are the use of resistors, metal oxide varistors and surge arrestors.

In this paper, we have proposed a novel hybrid-type superconducting DCCB model (SDCCB), in which a conventional hybrid DCCB (HDCCB) is combined with the SFCL. Superconducting fault current limiter (SFCL) is an application of superconductivity concept. There are two types of SFCL, resistive and inductive. This paper will elaborate and discuss the advantages of resistive SFCL combine with hybrid DCCB over other topologies like LC circuit based DCCB, solid state DCCB and conventional Hybrid DCCB.

2. PROCEDURE FOR PAPER SUBMISSION

Challenges: - HVDC transmission is associated with low DC reactance hence fault current rise to uncontrollable level. Breaking this huge dc fault current is the greatest challenge for MTDC protection system. For this reason, the main focus of HVDC CB research is on the mechanism of current zero creation across the interruption unit. So the main purpose of this topic is to study about the difference between AC and DC fault current level & getting knowledge by analysis & simulation of artificial current zero by different methods. The main objective of this paper is to develop a new topology for HVDC circuit breaker that eliminates use of any mechanical part or MOV.

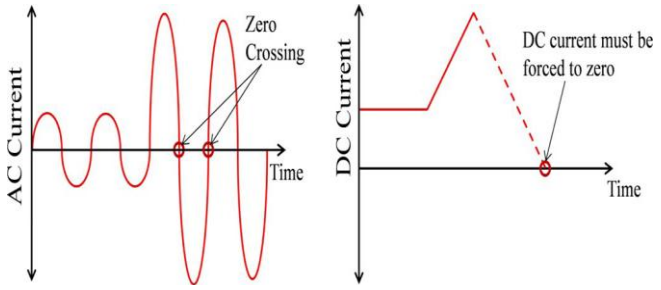

Fig - 1: Differences between AC and DC fault currents [4]

AC circuit breakers interrupt the ac fault current at its natural zero crossing, but there is no zero point in the dc fault current, as shown in Fig. 1. Therefore, DCCBs require an active method for reducing the current to zero level before breaking the circuit. Forcing the huge and rising dc fault current to zero in HVDC systems requires methods, which are very different from conventional ac circuit breakers [4]. The three methods commonly used to make zero dc fault current are Divergent current oscillation method, Inverse current injection method, and Inverse voltage generating method. In divergent current oscillation method, the current zero is made by high-frequency oscillating dc fault current until it touches the zero crossing, as shown in Fig. 2(a). This allow to use AC circuit breaker but this method is highly unstable because it uses large capacitors and inductors to create resonance condition. In addition, selection of components for its implementation depends mainly on network parameters such as line impedance and load. Therefore, a circuit breaker utilizing this method needs to be modified every time if any change in the HVDC system. In Inverse current injection method creates current zero by superimposing a high-frequency inverse current on dc fault current. It can be achieved by discharging a pre-charged capacitor, as shown in Fig. 2(b).

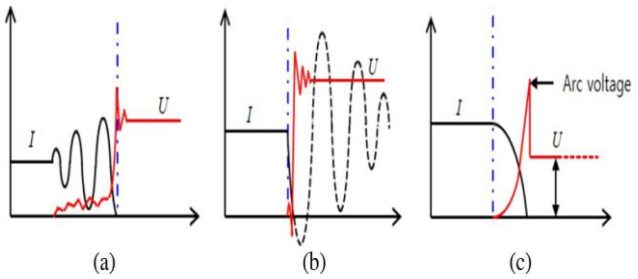

Fig - 2: DC voltage and current waveforms of commonly used methods for dc fault current interruption in dc switchgear. (a) Divergent current oscillation method. (b) Inverse current injection method. (c) Inverse voltage generation method [4]

This method results in a complex circuit breaker topology with large number of components and also requires an auxiliary power source to charge the capacitor. Third method is Inverse voltage generating method; in which current reduce to zero by making the arc voltage higher than the source voltage, as shown in Fig. 2(c). The inverse arc voltage in the circuit breaker ignites the parallel-connected surge arresters, and the network energy is dissipated in these surge arresters, and help to reduce the dc fault current to zero. In this paper, we investigated application of resistive SFCL on the HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL is one of good solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [4]. In order to analyze the performance of combined-application of SFCL on hybrid HVDC CBs, simulation studies were performed using MATLAB/Simulink and it is compared with conventional Hybrid HVDC system without SFCL.

Table - 1: Simulation Parameters

Fault Time	at 60 secs to 85 secs
Load data	150 ohm
Line length	200Km
AC system voltage	200 KV RMS
Power rating for normal system	2 GVA
Power rating for strong system	4 GVA
Power rating for very strong system	6 GVA

3. MODELLING AND SIMULATION

3.1 Conventional Hybrid HVDC Circuit Breaker

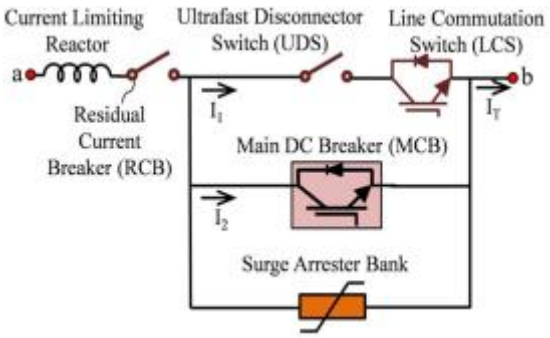

Fig - 3: Differences between AC and DC fault currents [4]

Simulation Circuit & results of the above single line diagram is shown in fig. 4 and fig. 5 respectively.

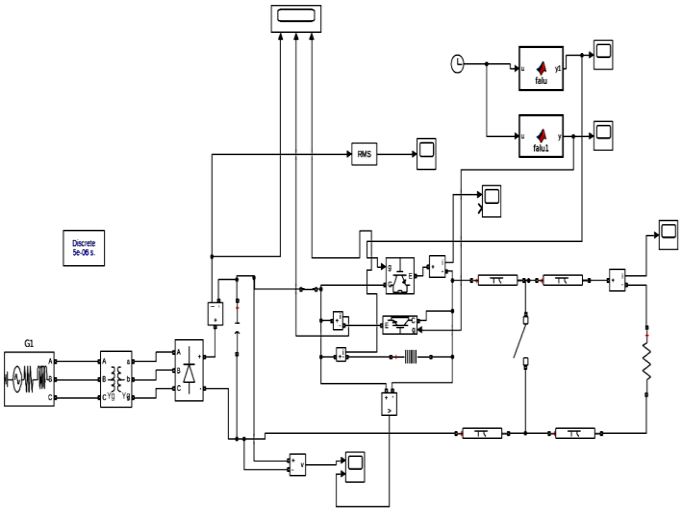

Fig - 4: Simulation of HVDC Mono polar System with conventional Hybrid HVDC Circuit Breaker

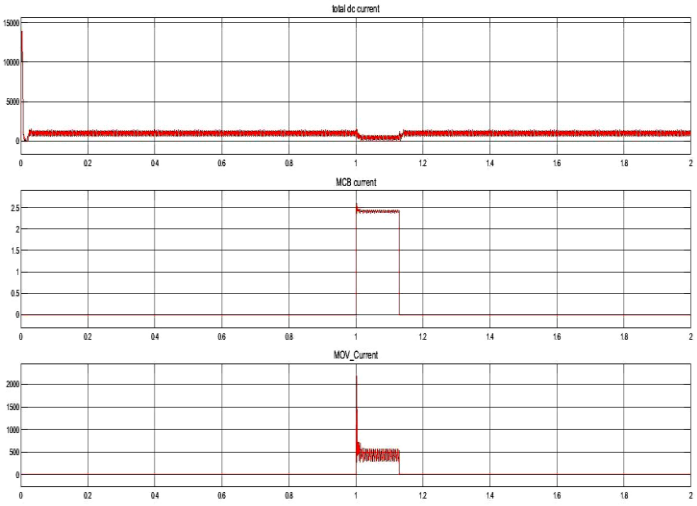

Fig - 5: Current in Various components of Hybrid Circuit Breaker

3.2 HVDC system with proposed SDCCB System

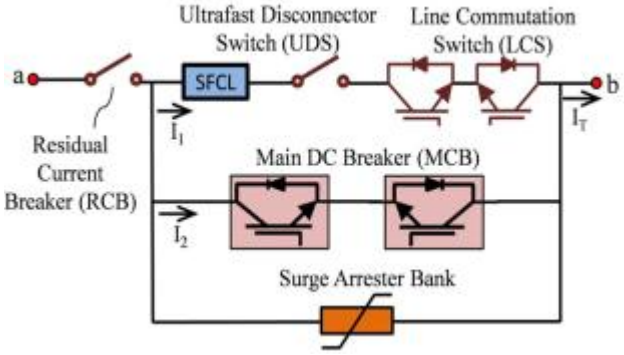

Fig - 6: Single-line diagram of proposed SDCCB with SFCL

Fig. 6 shows the proposed SDCCB, which is the modification of HDCCB in Fig.3. Modifications include the following: (1) the SFCL [8] is placed in series of the main current path (I1); (2) the series reactor has been removed since it is not needed anymore for current limiting; and (3) the single IGBT valve has been replaced by mirrored pair IGBT valves. The single IGBT valves in the HDCCB can only interrupt current in a single direction, i.e., from a to b in Fig.7(a) [4]. But reverse current continues to flow from the IGBT antiparallel diode. Fig. 7(b) shows the mirrored pair configuration of IGBTs.

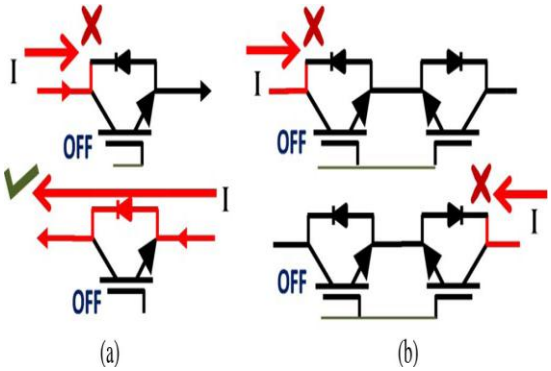

Fig - 7: (a) Single IGBT unable to break current in the reverse direction. (b) Mirrored pair IGBT configuration breaking current in both directions [4]

This arrangement of IGBTs will break the current independent of the direction of current flow. By considering above modification other MATLAB simulation is done which include combination of resistive SFCL and conventional Hybrid DCCB. Simulation circuit is shown in fig 8(a) and fig 8(b).

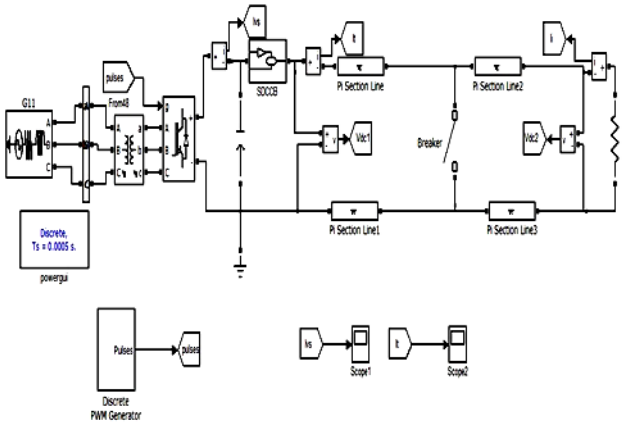

Fig - 8: (a) Main proposed system HVDC with SDCCB

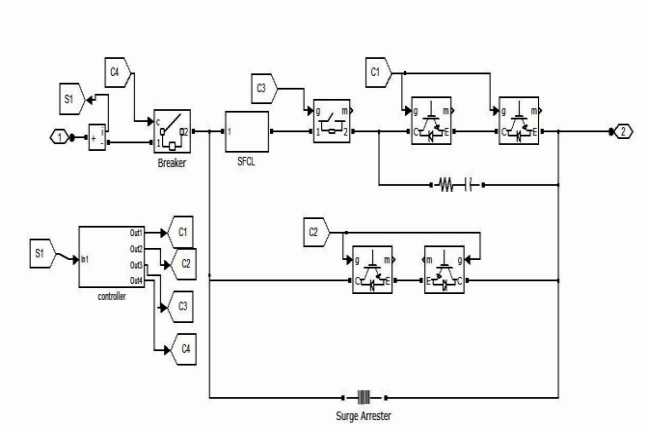

Fig - 8: (b) Main proposed system HVDC with SDCCB

The main objective of SFCL in SDCCB is to suppress the dc fault current to a lower level and also reduce the current interruption stress on SDCCB components. The SFCL will reduce the high dc fault current by inserting additional impedance ZSFCL in the circuit. [8,9]. The dc fault current intensity in the test model is dependent on the power rating of the ac system attached with the VSC-HVDC converter station. Three categories of ac power systems are used, which are denoted as "Normal System," "Strong System," and "Very Strong System." The corresponding fault currents due to these systems are marked as in, I_s, and I_{vs}, respectively. The type of AC systems, their power ratings, and fault current abbreviations are summarized at the end [4].

3.3 Simulation Results

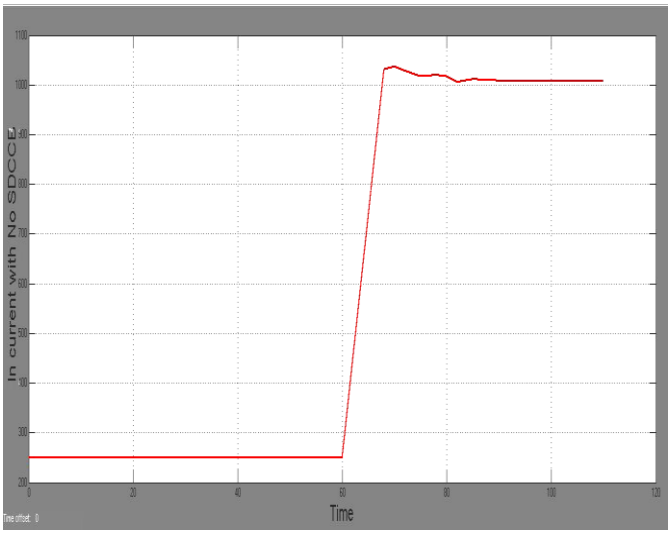

Fig - 9: (a) I_n (fault current for normal AC system) without SDCCB is 1000 A or 1 KA

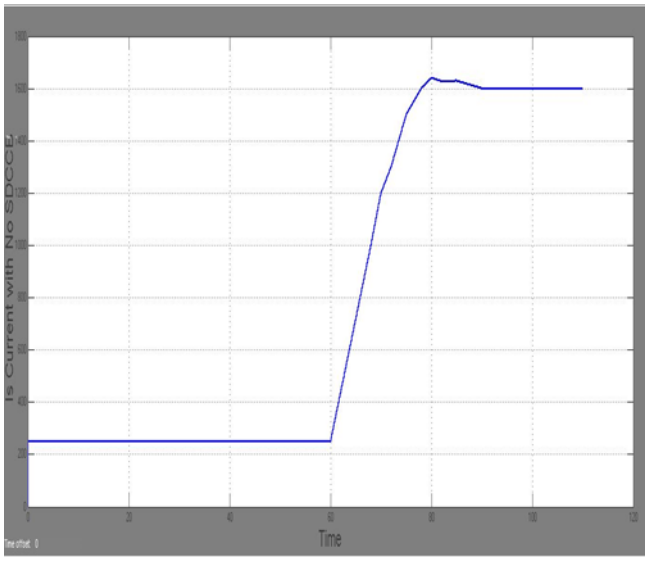

Fig - 9: (b) I_s (fault current for strong AC system) without SDCCB is 1600 A

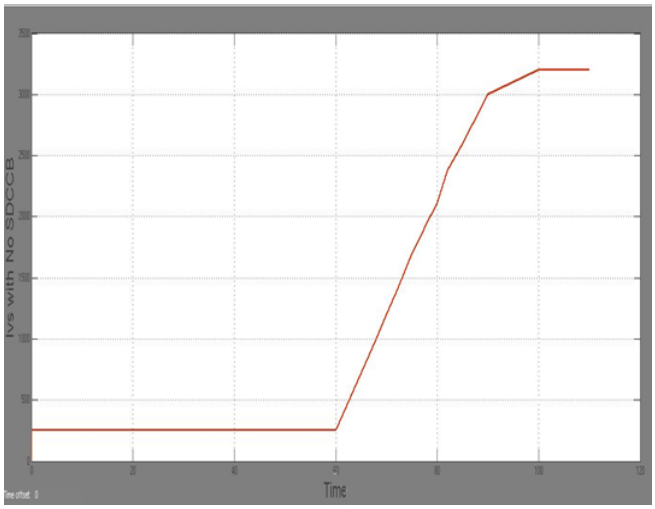

Fig - 9: (c) I_{vs} (fault current for Very strong AC system) without SDCCB is 3200 A or 3.2KA

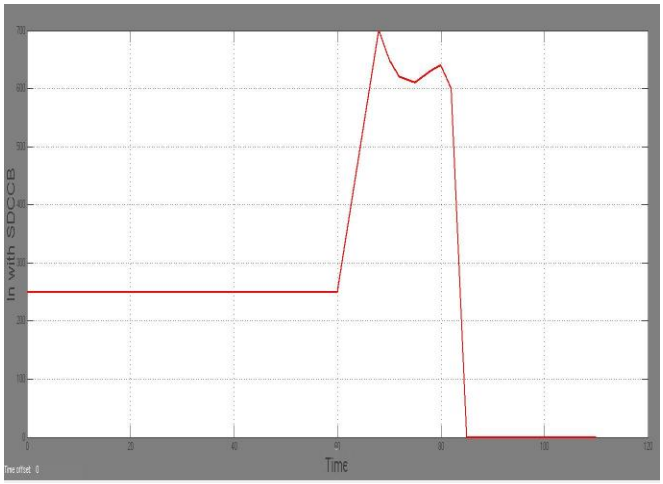

Fig – 10: (a) I_n with SDCCB is 705 A

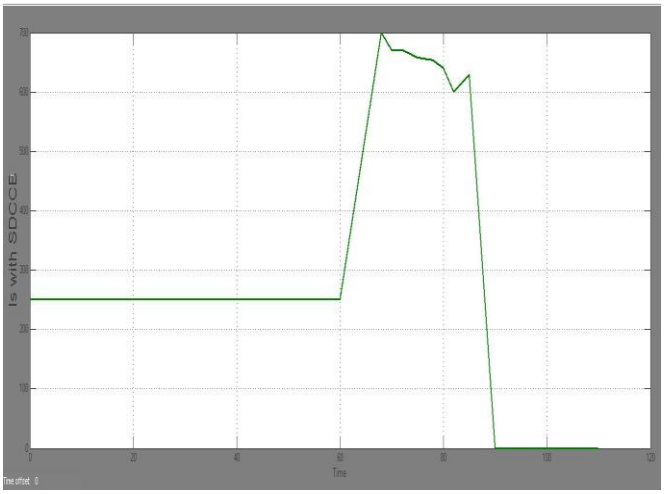

Fig – 10: (b) I_s with SDCCB is 700 A

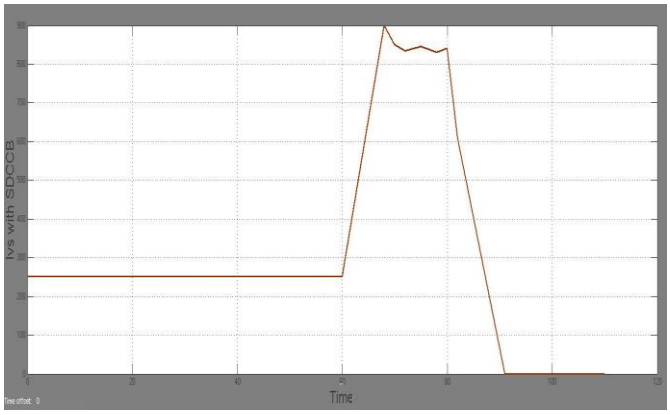

Fig – 10: (c) I_{vs} with SDCCB is 900A

The fault current rise to very large values if SFCL is not added in system but if SFCL is inserted in a system fault current reduced significantly. Table 2 summarizes the percentage reduction in dc fault current, which is being interrupted after application of SDCCB. Due to the SDCCB, the dc fault current reduced at considerable level, and this will significantly decrease the ratings and size of SDCCB components. Consequently, the cost of the SDCCB would decrease.

Table - 2: Percentage reduction in fault current for Changing fault current intensity

Fault Current Intensity with 2/4/6 GVA AC power rating	Total Current It with No SDCCB (A)	Total Current It with SDCCB (A)	Percentage Reduction in Fault current (%)
I_n (2GVA)	1000A	705A	29.50 %
I_s (4 GVA)	1600A	700A	56.25 %
I_{vs} (6 GVA)	3200 A	900A	71.88 %

4. CONCLUSION

Simulation result analyze in this paper clearly demonstrate fault current limiting capacity of resistive SFCL when it is combine with conventional Hybrid DCCB. This analysis suggest that proposed SDCCB is one of promising solution of issue in concern with the DC fault current limiting in HVDC system over several other topologies discussed in literature. During the fault current suppression stage, the intensity of the fault current reduced by SDCCB is depend on impedance added in SFCL. In future this analysis can be expand to check the behaviour of SDCCB with different values of ZFCL

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