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TCAD Simulation of Nano-Scale in AlN/GaN High Electron Mobility Transistor for High Power Millimeter Wave Applications

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Abstract - *The DC and microwave characteristics of $L_g = 20\,nm$ gate length depletion mode (D-mode) $InAlN/GaN$ High electron mobility transistor ($HEMT$) on SiC substrate with heavily doped source and drain region have investigated using Synopsys TCAD tool. The device having the features of recessed T - gate structure, InGaN back barrier and Al_2O_3 passivated device surface. The proposed HEMT exhibits a peak drain current density of $3\,[A/mm]$, transconductance g_m of $1600\,[mS/mm]$, current gain cut-off frequency f_t of $455\,GHz$ and power gain cut-off frequency f_{max} of $445\,GHz$. At room temperature the measured carrier mobility(μ) , sheet charge carrier density (n_s) and breakdown voltage are $1580\ (cm^2/V-s)$,$1.9\,X10^{13}\ (Cm^{-2})$ and $10.7\,V$ respectively. The superlatives of the proposed $HEMTs$ are bewitching competitor for future sub-millimeter wave high power RF VLSI circuit applications.*

Key Words: **HEMT, back-barrier, Recessed gate, cut-off frequency and short channel effects**.

1. INTRODUCTION

The preeminent physical property of GaN such as larger band gap ($3.44\,eV$) , breakdown field ($3.3X10^6 V/cm$), higher saturation velocity ($2.7X10^7 Cm/s$), good thermal conductivity ($1.95\,WCm^{-1}c^{-1}$) and higher mobility ($\mu_n = 2000$ *and* $\mu_h = 200\,Cm^2/V-s$) has captivated the raptness attentions to develop high power, high frequency very large scale integration ($VLSI$) circuits for next generation RF applications such as broadband communications, high power amplifiers for space research, microwave image sensing and low noise wide bandwidth amplifiers design . In the last two decade's several research progresses have been made to enhance the DC and Microwave characteristics of GaN based $HEMT$ [1-36]. Initially $AlGaN/GaN$ based $HEMTs$ are developed for high power applications such as solid state power amplifiers and high power switching applications [1-6]. To extent the operating frequency of the GaN based $HEMTs$ for sub milli-meter wave applications its necessary to scale down the device dimension, sub 50 nm gate length (Lg) , very thin barrier thickness ($< 15\,nm$), less than $1\,\mu m$ drain to space separation. The thinner barrier layer with $Al-rich\ AlGaN/GaN\ HEMTs$ are induced strain related issues at the interface between AlGaN/GaN due to lattice mismatch [7-10] and the ultra-scaled (below $50\,nm$) $AlGaN/GaN\ HEMTs$ are failed to reduce the short channel effects [10] due to poor aspect ratio (gate length to gate-channel separation) Lg/d.

The lattice matched $In_{0.17}Al_{0.83}N/GaN$ quantum well, reduced the strain related defects and achieved the maximum drain current of $3.3\,[A/mm]$ which is 205% higher than the $Al_{0.2}Ga_{0.8}N/GaN$ [11], because of its larger polarization induced charge carrier density ($\sim 10^{13} cm^{-2}$) in the two dimensional electron gas ($2DEG$) region. In recent years $InAlN/GaN\ HEMTs$ captivated enormous attention for high power sub-millimetre wave RF applications because of its good thermal stability, high current cut-off frequencies, minimum short channel effects and minimum leakage current with improved on/off ratio [15-26]. The higher cut-off frequencies (f_t *and* f_{max}) are achieved in $InAlN/GaN$ based $HEMTs$ by empowering aggressive scaling of device dimension with minimum gate leakage current, suppressed short channel effects ($SCEs$) and higher carrier mobility [15-26]. The key factors to improve the RF performances of $HEMTs$ with high power are minimum the gate access resistance (R_g), gate capacitances (C_{gd} *and* C_{gs} and fringing capacitances), low contact resistances, improved sheet resistance (R_{sh}) and high electron mobility in the channel. The aforementioned factors are achieved by various techniques such as ultra-scaled device dimension [21], recessed T- gate [23] , heavily doped source/drain regions (regrown ohmic contacts) [12], back barrier [19], spacer layer [20] and surface passivation[23].

A $80\,nm$ gate length SiN passivated T gate $InAlN/GaN\ HEMT$ on SiC manifested a maximum f_t/f_{max} of $114/177\,GHz$ [18]. The ultra scaled $30\,nm$ gate length conventional rectangular gate $InAlN/GaN\ HEMT$ with $InGaN$ back barrier demonstrated a record current gain cut-off frequency of 300 GHZ with minimum short channel effects ($SCEs$) [19]. The Al_2O_3 passivated $30\,nm$ conventional rectangular gate length $InAlN/GaN\ HEMTs$ had shown a cut-off frequency of 245 GHz, further the gate leakage current is reduced by oxygen plasma treatment [33]. The heavily doped source/drain region $n+\ GaN$ regrown ohmic contacts with $30\,nm$ conventional rectangular gate $InAlN/GaN\ HEMTs$ obtained a cut-off frequency (ft) *of* $370GHz$ with improved drain current density of 1.5 $[A/mm]$ and on/off ratio of more than six order of magnitude, however high $SCEs\,(DIBL)$ is observed [20]. A 25 nm thickness Al_2O_3 passivated T-shaped recessed gate length of $0.15\mu m$ $InAlN/GaN$ $HEMTs$ grown on SiC substrate and it demonstrated a peak transconductance of 675 $[mS/mm]$, peak drain current of 1.5 $[A/mm]$, f_t/f_{max} of 65/87 GHz [23]. Gate recessed SiN passivated 150 nm length T shaped gate enhancement mode $InAlN/AlN/GaN$ had shown a peak drain current density of 1.9 $[A/mm]$ and g_m of 800 $[mS/mm]$ with high on/off of 10^7 [24]. The enhanced carrier confinement, higher mobility1300 $(cm^2/V-s)$, improved sheet resistance R_{sh} of 420 $[ohm/Sqr]$ with reduced buffer leakage is demonstrated by using 3nm $InGaN$ back barrier in [18].

In this article, we have proposed and investigated the DC and microwave characteristics of a novel 20 nm heavily doped $(n+GaN\,\&\,n+InGaN)$ regrown ohmic source/drain regions with recessed T-gate $InAlN/AlN/GaN$ $HEMT$. To obtain the superior carrier confinement in 2DEG with enhanced carrier mobility $In_{0.15}Ga_{0.85}N$ is used as back barrier in our model. The parasitic gate capacitances are majorly suppressed by Al_2O_3 passivation. The higher aspect ratio is maintained (Lg/d) by recessed gate structure to effectively reduce the short channel effects. The proposed novel $Lg = 20\,nm$ $InAlN/GaN$ $HEMT$ device shows an excellent improvement in DC and RF characteristics. The maximum drain current density I_d of 3 $[A/mm]$, a record g_m of 1600 $[mS/mm]$, f_t of 455 GHz and f_{max} of 445 GHz recorded. The gate leakage current and $SCEs$ are majorly suppressed and improved on/off ratio is achieved. These high DC and RF performances of the $HEMT$ obtained because of extreme reduction in the device parasitic resistances and capacitances with high sheet charge carrier density and mobility in 2DEG channel.

2. DEVICE STRUCTURE AND BAND GAP DIAGRAM

The vertical cross section of $InAlN/AlN/AlN$ $HEMT$ device structure is depicted in Fig-1. The device consists of 3 $inch$ SiC substrate to achieve good thermal stability,1450 nm Fe doped GaN buffer layer which isolate the channel from the substrate defects, 3.5 nm $InGaN$ back barrier layer which helps to confine the more electron in the channel due its effective conduction band notch at the interface with GaN channel and also it contributed for higher carrier mobility in the 2DEG $(\sim 1500\,cm^2/V-S)$. Moreover the buffer leakage current is suppressed by the $InGaN$ back barrier. The channel region is defined by 30 nm GaN and 10 nm $In_{0.17}Al_{0.83}N$ is used as barrier layer. A very thin 1nm AlN spacer layer is placed between the barrier and channel which improves the electron mobility in the 2DEG by reducing the interface roughness and alloy disorder scattering at the interface of $InAlN/GaN$.The induced spontaneous and piezoelectric polarization electric field provides an improved sheet charge carrier density of $1.9X10^{13}cm^{-2}$ in the 2DEG and also due to the higher band gap of the barrier limits the gate leakage current and mitigates the short channel effects in the device. The source and drain regions are formed by heavily doped GaN (50 nm) with Si in the order of $\sim 7X10^{20}cm^{-3}$ to minimize the contact resistances. The source and drain ohmic contacts were designed by using $Ti/Pt/Au$ metal stack and T shaped recessed gate is formed by Pt/Au metal stack. T-gate structure having the head size of 400 nm, stem height of 140 nm with 20 nm footprint is designed, which liftoff wide cross sectional gate area with smaller gate length and schottky contact is formed by $Ni/Pt/Au$ metal stack. The drain to source separation is kept at 100 nm. In order to reduce the parasitic capacitances of the device, finally the device surface is fully passivated by 10 nm Al_2O_3layer which greatly helped for achieving higher cut-off frequencies. Usually Si_3N_4 is the commonly used passivation layer to avoid the current collapses, but the larger thickness of passivation layer is needed, which will increases the gate capacitance particularly gate-drain capacitance (Cgd) . In this model a 10 nm Al_2O_3 is used as passivation layer which assists to unfasten the dispersion effects and it provides a root to good transport property in the 2DEG [36].

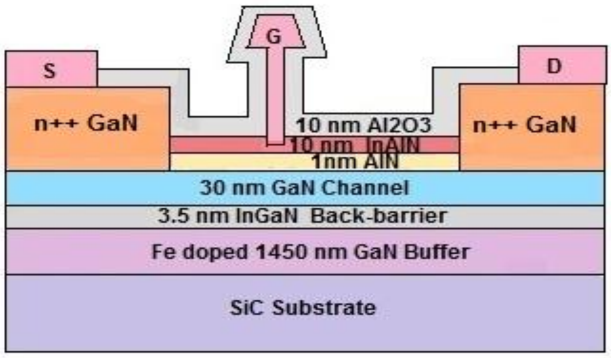

Fig-1: Vertical cross section of Lg 20 nm $InAlN/AlN/GaN$ $HEMT$ $with$ $InGaN$ $back-barrier$

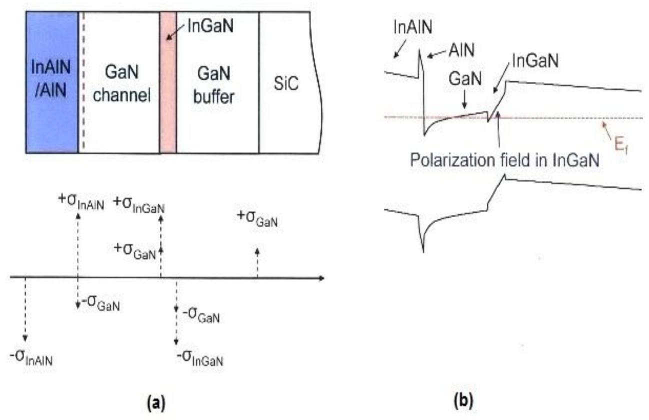

Fig-2: Polarization charge distribution and Conduction band offset of $InAlN/AlN/GaN\ HEMT$ with $InGaN$ Back barrier.

The Polarization charge distribution and conduction band offset diagram of $InAlN/AlN/GaN/InGaN$ is depicted in Fig-2.a and Fig-2.b respectively. Due to induced piezoelectric polarization between $InGaN\ and\ GaN$ there will be a sharp raised potential barrier is formed at the back of $2DEG$ channel. Such a sharp notch helps to confine the electron in better manner in the channel region and also it mitigates the buffer leakage current. A thin 1 nm wide band gap (6.01 eV) AlN spacer layer offers large effective conduction band offset and also it helps to reduce the gate leakage current.

3. RESULT AND DISCUSSION

Chart-1 shows the sheet charge carrier density variation with $InAlN$ barrier thickness. The higher the thickness of barrier layer gives better sheet charge density. In this work a 10 $nm\ InAlN$ barrier layer offered a sheet carrier density of $1.9\ X10^{13}\ Cm^{-2}$ and obtained carrier mobility of electron in the $2DEG$ is 1580 $cm^2/V-s$.

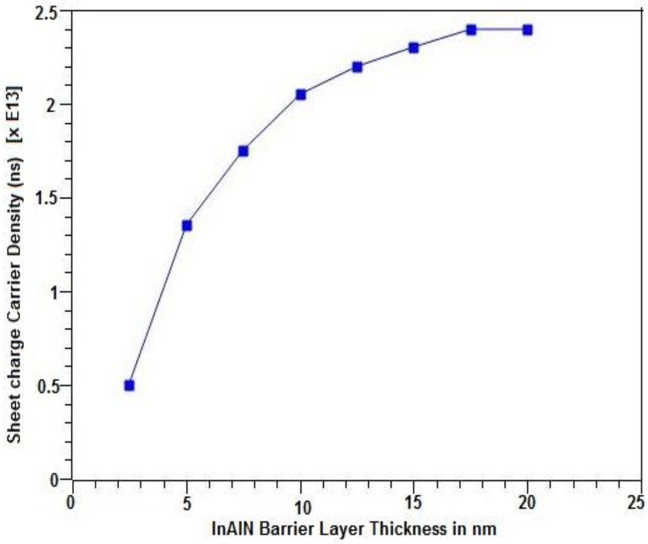

Chart-1: 2DEG sheet charge density dependency on barrier layer thickness

Chart-2 shows the $V-I$ characteristics of $L_g = 30\ nm$ and $w = 2X40\ \mu m\ D - mode\ InAlN/AlN/GaN\ HEMT$. The simulation result gives a supreme drain current of 3 $[A/mm]$ at $V_{gs} = 2V$ and the device is pinched off perfectly at $V_{gs} = -2V$. The extracted very low on resistance (Ron) of the device for $V_{gs} = 2V$ is 0.26 $ohm - mm$. This higher current density is achieved mainly because of the enhanced mobility with greater sheet charge carrier density in $2DEG$ channel. The lattice matched $InAlN/GaN$ with 1 $nm\ SiN$ spacer provides effective conduction band offset and it reduces strain induced surface defects at the interface. Moreover the $InGaN$ notch helps to provide the better confinement of charge carrier in channel and also it suppressed the buffer leakage current in the device. A 10.7 V off state breakdown voltage is obtained by varying the gate-source potential depicted in Chart-3 for $I_{ds} = 10mA/mm$ and the corresponding gate-drain breakdown field of $\sim 2.6MV/cm$.

Chart-4.a shows the transconductance variation with the gate bias voltage. The maximum transconductance of the device is extracted from the plot is 1.6 $(S/mm)\ at\ Vgs = -0.8V$ and the associated drain current I_{ds} of 0.9 A/mm. The extracted threshold voltage of the device from the transfer characteristics Chart-4.b $(Ids - Vgs)\ is\ -1.4V$. The subthreshold and gate leakage current characteristics of L_g = 20 nm and $w = 2X40\ \mu m\ D - mode\ InAlN/AlN/GaN\ HEMT$ is shown in Chart-5. The gate leakage current is depends on band gap of the barrier and channel materials. The higher band gap $InAlN\ with\ AlN$ space layer effectively suppressed the gate leakage current in the order of $1X10^{-12}\ A/mm$. The drain current on/off ratio is observed as 10^7 at $V_{ds} = 2V$.

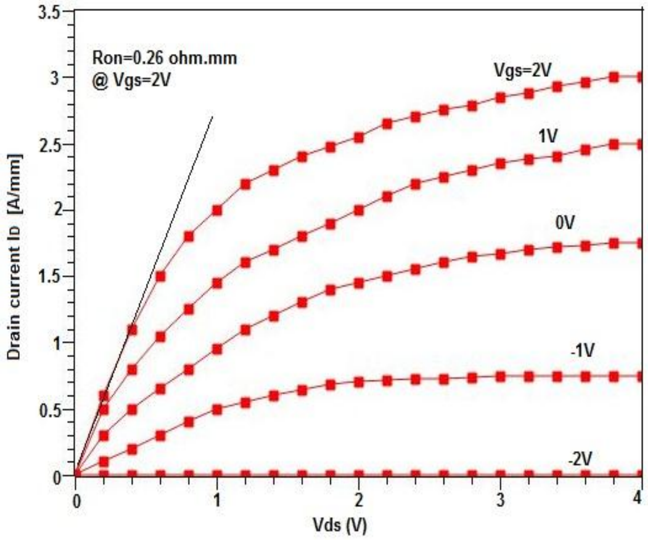

Chart-2: V-I Characteristics of L_g = 20 nm and $w = 2X40\ \mu m\ D-mode\ InAlN/AlN/GaN\ HEMT$

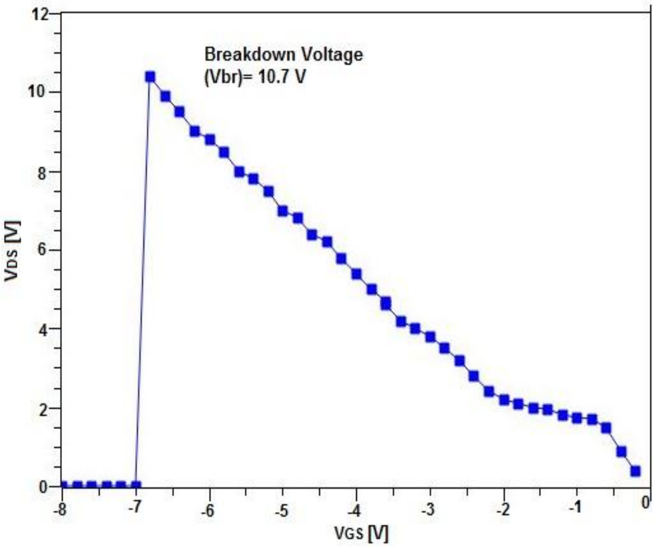

Chart-3: $V_{gs} - V_{ds}$ breakdown sweeps with fixed drain current 10 mA/mm of L_g = 20 nm and $w = 2X40\ \mu m\ D-mode\ InAlN/AlN/GaN\ HEMT$.

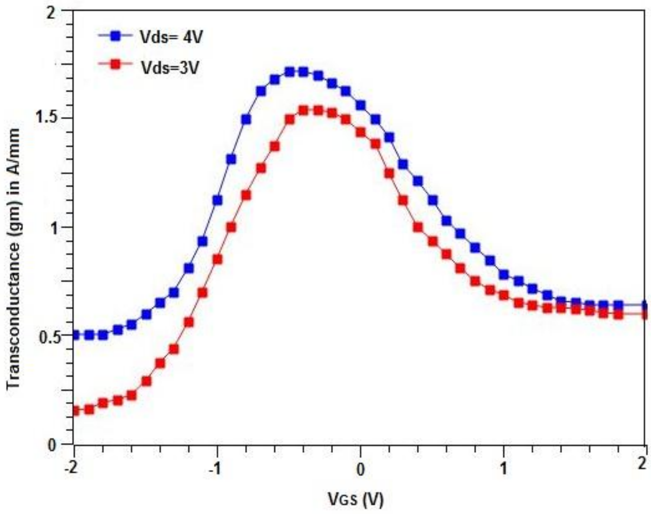

Chart-4.a: Dependences of g_m on the gate bias of L_g = 20 nm and $w = 2X40\ \mu m\ D-mode\ InAlN/AlN/GaN\ HEMT$.

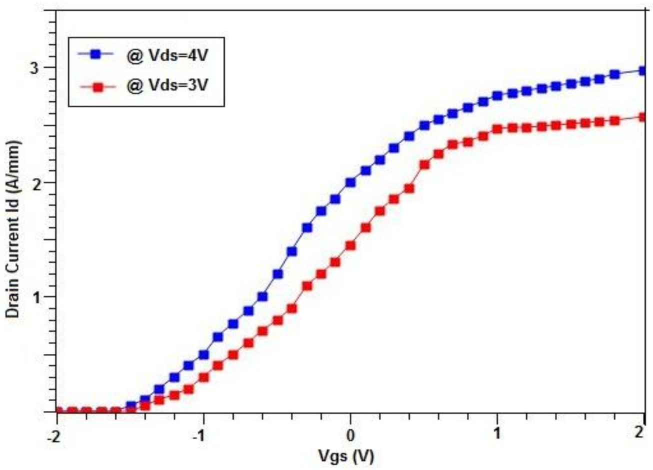

Chart-4.b: Dependences of I_d on the gate bias of L_g = 20 nm and $w = 2X40\ \mu m\ D-mode\ InAlN/AlN/GaN\ HEMT$.

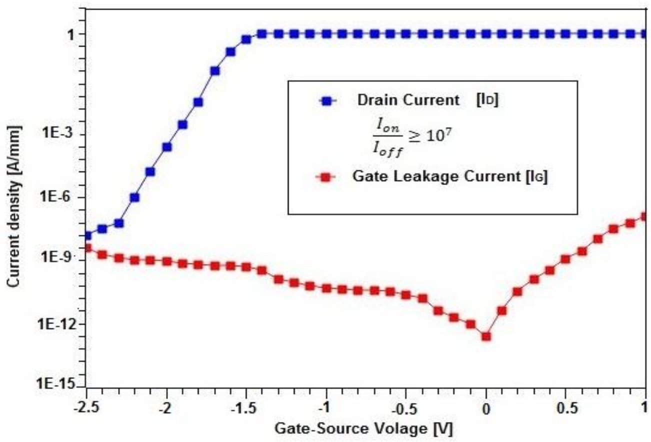

Chart-5: Subthreshold and gate leakage current characteristics of L_g = 20 nm and $w = 2X40\ \mu m\ D-mode\ InAlN/AlN/GaN\ HEMT$.

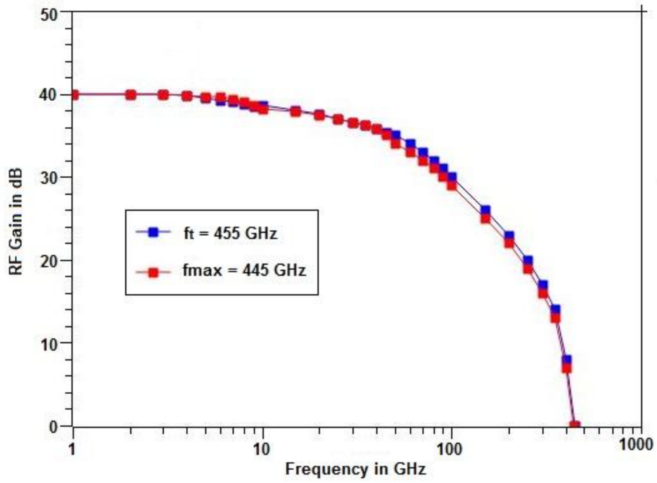

Chart-6:Cut-off frequencies Vs RF gain of L_g = 20 nm and $w = 2X40\ \mu m\ D-mode\ InAlN/AlN/GaN\ HEMT\ for\ Vds = 4V$.

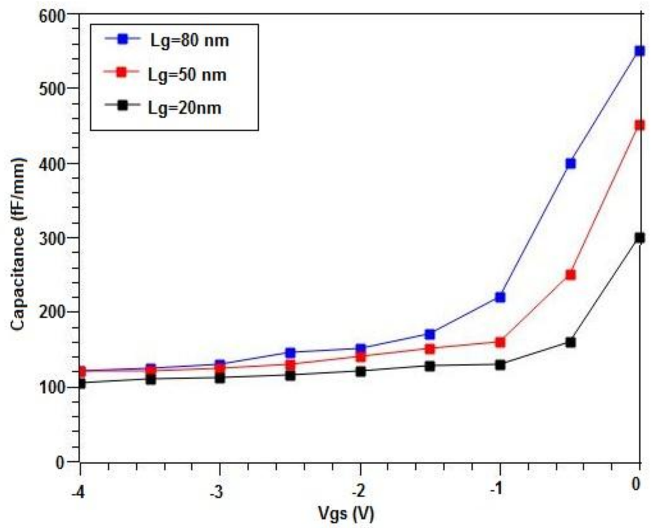

Chart-7: Gate length dependence on capacitance $(Cgs + Cgd)$ of the $InAlN/GaN\ HEMT$ under cold FET bias condition ($Vds = 0V$).

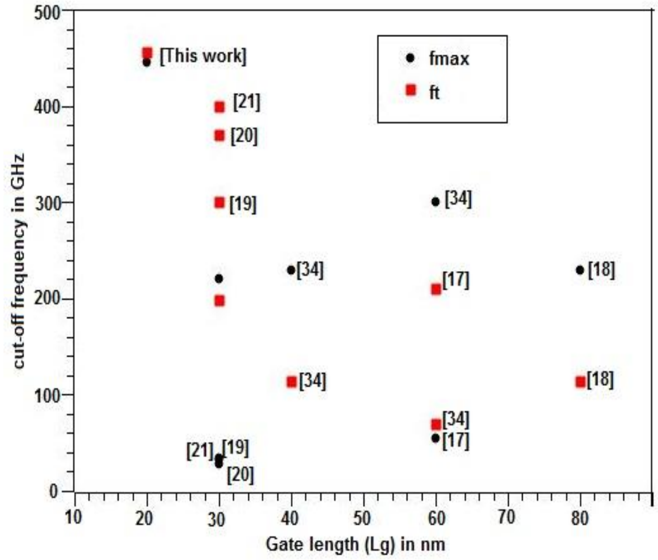

Chart-8: Comparison model of $InAlN/GaN\ HEMT$ simulation result with experimental data.

The simulated current gain cut-off frequency (ft) and power gain cut-off frequency $(fmax)$ of $Lg = 20\ nm\ InAlN/AlN/GaN\ D-HEMT$ are $455\ and\ 445\ GHz$ respectively. The obtained values are the best cut-off frequencies of depletion mode $InAlN/GaN\ HEMTs$ with peak drain current of $3\ [A/mm]$ and low gate leakage mechanism among any materials so far from author's knowledge. The higher $ft\ and\ fmax$ is achieved by drastic reduction in the contacts resistances and parasitic capacitance of the device mainly because of heavily doped $(n++GaNN)$ source / drain regions has direct contacts with the channel, combined with $\sim 50nm$ drain and source access region and passivated device surface. The features of recessed T-gate structure is suppressed the short channel effects $(SCEs)$, escalated transconductance (gm) and the attenuated drain conductance also contributed to achieve this higher $ft\ and\ fmax$. The RF gain versus cut-off frequency is depicted in Chart-6.

The expression for $ft\ and\ fmax$ are written as follows ;
Current gain Cut-off frequency:

$$f_t = \frac{g_m/g_{ds}}{2\pi\left(\left((C_{gs}+C_{gd})+\left(\frac{1}{g_{ds}+(R_s+R_d)}\right)\right)+(C_{gd}.g_m/g_{ds})(R_s+R_d)\right)}$$

Power gain cut-off frequency:

$$f_{max} = \frac{f_t}{2\sqrt{(R_s+R_g)g_{ds}+2\pi f_t R_g C_{gd}}}$$

Where the source resistance $R_s = \left(\frac{R_c}{w}\right) + \left(\frac{R_{sh}.L_{GS}}{w}\right)$ and drain resistance $R_d = \left(\frac{R_c}{w}\right) + \left(\frac{R_{sh}.L_{SD}}{w}\right)$. R_c is the contact resistance and R_{sh} denotes the and channel sheet resistance respectively. L_{GS} is gate to source distance and

L_{SD} is gate to drain separation respectively. w is the width of the gate. R_g is the gate access resistance and g_{ds} represents drain conductance. The gat to drain capacitance is C_{gd} is essential parameter for high frequency operation of the device. A 10 nm Al_2O_3 passivated device surface reduces the overall gate capacitance in our proposed device model. Chart-7 displays the extracted capacitance $(Cgd + Cgs)$ *of InAlN/GaN HEMT* under cold FET bias, i.e $Vds = 0V$. For higher the Vgs above the threshold voltage of the device $2DEG$ channel started charging causes the capacitances of the device increase rapidly and higher the value for longer gate length.

The extracted small signal parameters transconductance g_m, drain conductance g_{ds} , gate-source capacitance C_{gs} , gate-drain capacitance C_{gd} , source resistance R_s , drain resistance R_d, subthreshold slope (SS), Sheet resistance (Rsh) and on resistance (Ron) of the 20 nm recessed T gate *InAlN/AlN/GaN HEMT* device with heavily doped source and regions are 1.6 S/mm ,0.245 S/mm, 312 fF/mm, 107 fF/mm, 0.05 ohm-mm, 0.12 ohm-mm, 85 mV/dec, 420 ohm/sqr and 0.26 ohm-mm respectively. The comparison of our simulation result with various experimental results for different gate lengths is shown in Fig-10. and Table.1. *InAlN/GaN MOSHEMT* [21] exhibits a f_t of 400 GHz but the obtained f_{max} is 33 GHz only . In this work the proposed novel 20 nm *InAlN/GaN HEMT* shown a f_t/f_{max} of 455/445 GHz . These high cut-off frequencies with improved drain current density 3 A/mm, record transconductance (g_m) of 1050 mS/mm, high on/off ratio 10^7 and low gate leakage current $10^{-12} A/mm$ shown that the proposed *InAlN/AlN/GaN HEMT* will be a promising candidate for future forerunner of high speed and high power millimetre wave RF applications. In future the gate leakage current of the device further reduced by using a high dielectric insulator between the gate and barrier (*MOSHEMT/MISHEMT*).

4. CONCLUSION

The *DC and RF* characteristics of a novel 20 nm recessed T-gate *InAlN/AlN/GaN HEMT* with *InGaN* back barrier has been studied by using Synopsys T*CAD* . The simulation is performed by using physics based drift-diffusion model at room temperature. The device features are heavily doped $(n++)$ source/drain regions with Al_2O_3 passivated device surface which are helped us to reduce the contact resistances and gate capacitances of the device to uplift the microwave characteristics of the *HEMTs*. *Lg of* 20 nm *HEMT* Shows a current gain cut-off frequency of 455 GHz and power gain cut-off frequency of 445 GHz. The peak drain current density of 3 A/mm is achieved by offering effective conduction band offset by using *AlN* spacer associated with *InGaN* back barrier to enhance the sheet charge carrier density in $2DEG$ region $(1.9\,X10^{13}\,Cm^{-2})$ with higher carrier mobility of 1580 $(cm^2/V-s)$. The recessed T-gate structure reduced the short channel effects $(SS = 86\,mV/dec)$ by minimizing the gate to channel separation. The superior *DC and RF* performance of proposed *HEMT* device expected to be the most optimistic applicant for future high power millimetre wave *RF* applications.

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