International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 06 | June 2020 www.irjet.net p-ISSN: 2395-0072

Development of 40V Testing Capability for MAGNUM NEXTEST ATE

Hemanthkumar V[1], Rishabh Kumar D Jain[2], Namita Palecha[3]

[1]*Hemanthkumar V, Dept. of Electronics and Communication Engineering, RV College of Engineering, Bengaluru, Karnataka, India*

[2]*Rishabh Kumar D Jain, Dept. of Electronics and Instrumentation Engineering, M.S. Ramaiah Institute of Technology, Bengaluru, Karnataka, India*

[3]*Namita Palecha, Assistant Professor, Dept. of Electronics and Communication Engineering, RV College of Engineering, Bengaluru, Karnataka, India*

Abstract - *An Automated Testing Equipment is an apparatus which can test devices as per the instructions given to it. Usage of ATE at production level where millions of devices are tested has resulted in huge reduction in test time and human errors in testing. There are many factors where an ATE is chosen for a product. Few of them are test cost, parallelism, tester specification etc. Goal of testing is to ensure less test cost and less test time with high fault coverage. This can be achieved with proper choosing of an ATE as per product specification. In this work, the board design of AS1340 as a boost converter is developed to improve the tester specification. MAGNUM NEXTEST ATE which has Device Power Supply and High Voltage Channel can maximum drive 15V and 28V respectively to any connected Device pin. Anything above 28V cannot be driven by MAGNUM NEXTEST ATE. Hence as an additional feature to an ATE, AS1340 is integrated so that an ATE can drive 40V to any connected device pin.*

Key Words: *Automated Testing Equipment (ATE), Boost Converter, Semiconductor Testing, MAGNUM NEXTEST Tester, Device Power Supply (DPS) Tester Channel, High Voltage Tester Channel*

1. INTRODUCTION

The rapid growth in the complexity of devices and its performance has led to the improvement in the field of testing[1]. Semiconductor testing is an important stage in device manufacturing cycle. Any defects in the devices will be identified in this phase to make sure customers doesn't receive defective devices. But the issue with testing is that it increases device cost and time to market. Hence reduced test time and test cost are the challenges for test engineers without compromising on the testing quality. The shifting from manual testing to automatic testing[2] have been the most preferable way to reduce test time and improve fault coverage[3]. ATE has been used to test many different types of devices like memories[4], controllers, System on Chip (SOC)[5] etc.

Usage of ATE for testing of devices will work until the device specification are met by tester specification. When the complexity of a device increases and tester resources are not enough, change of an ATE or improvement to an existing ATE[1] are done. The former approach will surely increase the device cost because of the new ATE and implementing new setup environment which is time consuming. The later approach involves designing of external modules that will improve the testing capability of an existing ATE[6]. Multisite/ Concurrent testing[7-8] is one of the approaches used to reduce test time by efficiently utilizing tester resources. Usage of offline testers for setting up test environment and debugging small errors will improve test cost[9], because when online testers are used efficiently, test cost can be reduced. It is important to automatically update the test software and hardware to improve the efficiency of test results. Thus, techniques like imaging the tester[10] and analyze the requirement of software and hardware will be crucial to extract better results from an ATE.

2. Design of AS1340 for 40V testing capability

As mentioned in [6] using of external module to improve the specification of tester is carried out in this work. An ATE called MAGNUM NEXTEST TESTER's specification is improved to incorporate 40V testing of devices.

2.1 Details of MAGNUM NEXTEST ATE

The architecture of MAGNUM NEXTEST ATE is designed to support maximum of 64 Device Power Supplies(DPS) and 128 High Voltage(HV) channel. The specification of DPS and HV channel is shown in Table I and Table II respectively.

Table I Specification of DPS Channel

Parameter	Range	Resolution	Accuracy
Current	0 to 400mA	200uA	+/- 500uA+0.2% of Value
Voltage	-15 to 15V	5mV	+/-10mV

Table II Specification of HV channel

Parameter	Range	Resolution	Accuracy
Voltage	0 to 28V	2mV	+/-25mV
Current	0 to 8mA	4uA	+/- (20uA+0.2% of Value)

2.2 METHODOLOGY

To support 40V testing with maximum current of 30mA, a boost converter is used to generate 40V by taking in 5V and 330mA from the tester. Boost converter works on the principle of driving the load with both supply voltage and charged inductor. The charging of inductor is done in first cycle and driving of load happens in subsequent cycle. The duration of charging and driving cycle decides the stable output at the load.

2.3 Experimental Details

AS1340 is a boost converter which operates from a 2.7 to 5.5V supply and can produce output voltage up to 50V. The specification of AS1340 is described in Table III. The AS1340 board design is shown in Fig. 1.

Table III Specification of AS1340

Parameters	Values
Vout	2.7V to 50V
Vext	2.7V to 50V
Vcc	2.7V to 5.5V
Switching Frequency	1MHz
Output Power	1.08W to 1.2W
Maximum Efficiency	93%

AS1340 can be operated in two modes, VCC mode and EXT mode:

1. VCC mode- Connecting the input side of inductor to VCC via SWVIN and SWVOUT pins as shown in Fig. 2 by applying VCC potential to EN, i.e EN=1.
2. EXT mode- Connecting the input side of inductor to external supply of range 2.7V to 50V as shown in Fig. 3 by applying ground potential to EN, i.e EN=0.

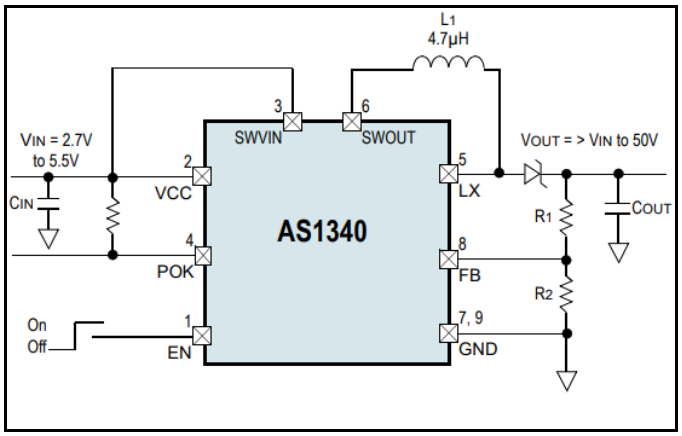

Fig 1. Board Design of AS1340

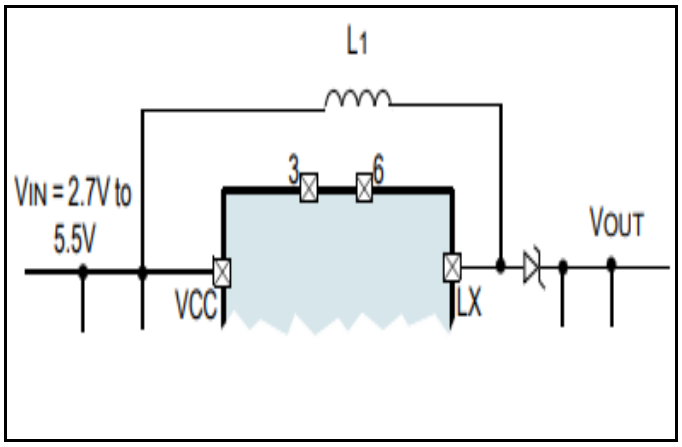

Fig 2. VCC Mode

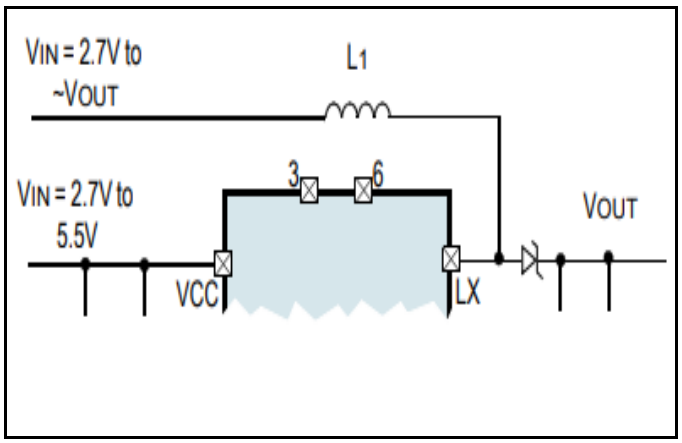

Fig 3. EXT Mode

Both these methods provide the same operation. But when input of inductor is handled independently as shown in figure 3, inductor can be charged with higher voltages (maximum of 50V), which decreases the charging time.

Hence, based on the application, AS1340 can be operated in two modes. In this work, VCC mode is used, as EXT mode requires an additional tester channel to drive inductor input.

figure 4 shows the interfacing design of AS1340 with 5V tester channel of ATE which can provide regulated 40V at the output.

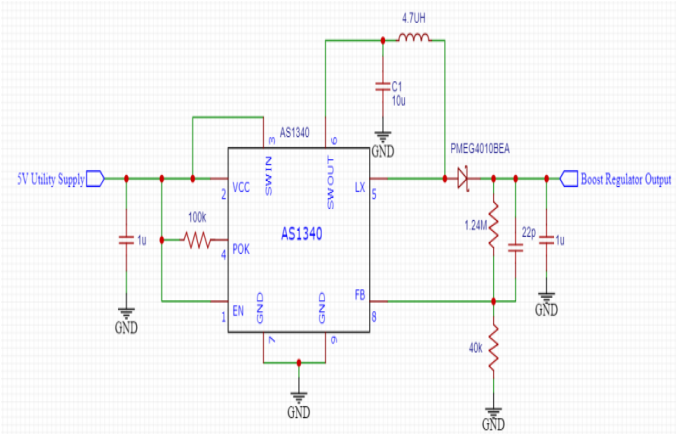

Fig 4. Interfacing design of AS1340 boost converter

Operation of AS1340 as boost converter is described below:

An input voltage of 5V is applied to the VIN pin of AS1340. Initially, one end of inductor (4.7uH in figure 4) is connected to supply voltage via SWVIN and SWVOUT pin (together called as SW pins) and another end of inductor (4.7uH in figure 4) is connected to GND via LX pin. Upon this connection, inductor gets charged to a sufficient level where it can establish regulated 40V at the output. This duration is called as charging cycle. Later, the other end of the inductor (4.7uH in figure 4) which was connected to GND earlier will be connecting to external resistor divider via diode. Now the output of boost converter will be supplied from VIN as well as voltage across inductor and establishes 40V at the output. This duration is called as driving Cycle. The switching between charging and driving cycle will happen based on the feedback voltage coming in from the resistor divider network at the output. The output voltage of 40V will result in suitable feedback voltage which is then compared with the comparator inside AS1340. Based on the output of comparator, duration of charging cycle and driving cycle will be modulated. The output voltage of AS1340 is given by Equation-1.

$$Vout = 1.25 * (1 + \frac{R12}{R11}) \quad (1)$$

Where,
R12 is the resistor between output pin and FB pin.
R11 is the resistor between FB pin and GND.
Vout is the output of boost converter.

Bypass capacitor at the input is used to eliminate noise as per pin description of AS1340. Output capacitor is connected for the purpose of stability.

3. Results and Discussions

The design shown in figure 4 is implemented with the generic load board of an ATE for the supply of 5V and the output voltage is measured with multimeter.

Figure 5 shows the AS1340 evaluation board. Figure 6 shows the Generic load board that can drive 5V and 330mA of supply to AS1340.

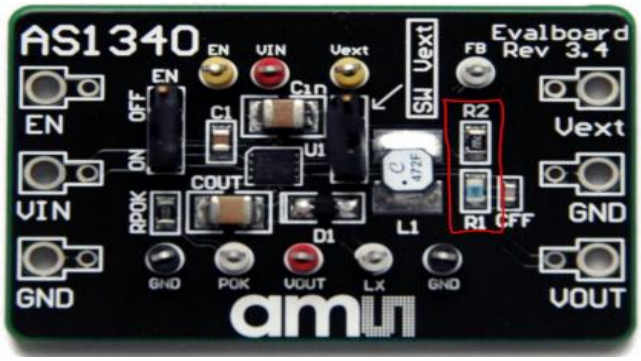

Fig 5. AS1340 Evaluation Board

Fig 6. Generic Loadboard of ATE

Figure 7 shows the supply voltage of 5V and 330mA of current. Figure 8 shows the connection of generic load board being connected as input and 40V measured from the multimeter at the output. Figure 9 shows the output voltage and output current of AS1340 evaluation board.

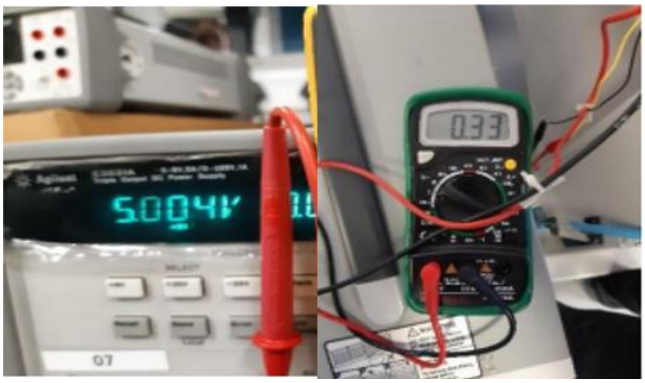

Fig. 7. Supply for AS1340

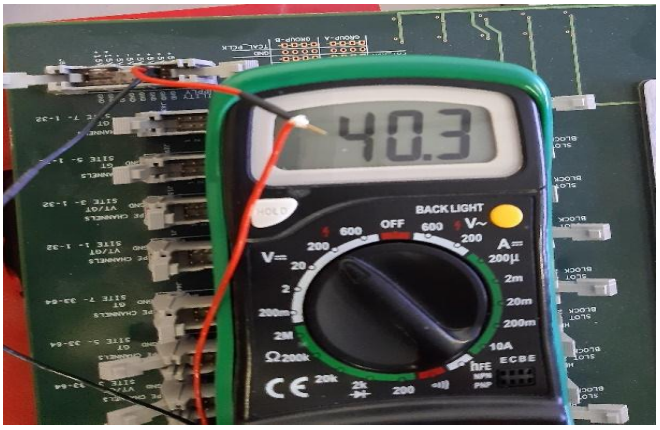

Fig 8. Connection of loadboard with AS1340

Fig 9. Output of AS1340

Inference: As per the results obtained above when input of 5V and 330mA of current is driver from tester to AS1340, an output of 40V with 30mA of current was observed at the output of boost converter. Also, the power input and power output were found to be 1.65W and 1.2W, leading to the efficiency of this design to 72.72%. The result obtained in presented in table IV.

Table IV Experimental Results on AS1340 as boost converter

Parameter	Value
Input Voltage	5V
Input Current	332 mA
R12	1.24MΩ
R11	40KΩ
Output Voltage	40V
Output Current	30mA
Efficiency	72%

4. CONCLUSIONS

The board design of AS1340 is done. The AS1340 is operated in VCC mode to avoid an additional tester channel from an ATE required in EXT mode. Both SWIN and SWOUT pins were active in the charging cycle to charge the inductor.

The value of R12 and R11 is chosen as per the equation 1 to generate any voltage between 2.7V to 50V at the output. In this work, R12 is set to 1.24MΩ and R11 is set 40KΩ to generate 40V at the output of boost converter. Finally, when input supply of 5V is driven to AS1340, 40V at the output of the converter is measured.

Since the designed values were verified correctly and no damage happened to either design or an ATE. AS1340 can be used as a boost converter to provide 40V testing capability for a MAGNUM NEXTEST ATE.

ACKNOWLEDGEMENT

We thank Cypress India Test team for providing an opportunity to conduct this experiment on their MAGNUM NEXTEST ATE and for their suggestions throughout this experiment.

REFERENCES

1. B. G. West, "Advanced Test Methodology and Strategies for Semiconductors," 2006 13th International Symposium on the Physical and Failure Analysis of Integrated Circuits, Singapore, 2006, pp. 119-124.
2. S. E. Thomas and P. R. Nishanth, "Development of automated test equipment for ESP controllers," 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, 2017, pp. 869-872.
3. (2006) Automatic Test Equipment (ATE) and Production Test. In: Integrated Circuit Test Engineering. Springer, London.
4. P. Pellati and P. Olivo, "Automated test equipment for research on nonvolatile memories," in IEEE Transactions on Instrumentation and Measurement, vol. 50, no. 5, pp. 1162-1166, Oct. 2001.
5. Kramer, R. (2004). ATE for SOC multisite testing. EE, Evaluation engineering. 43. 18-+.
6. R. Rajsuman, N. Masuda and K. Yamashita, "Architecture and design of an open ATE to incubate the development of third-party instruments," in IEEE Transactions on Instrumentation and Measurement, vol. 54, no. 5, pp. 1678-1698, Oct. 2005.

7. T. Nakajima, T. Yaguchi and H. Sugimura, "An ATE architecture for implementing very high efficiency concurrent testing," 2012 IEEE International Test Conference, Anaheim, CA, 2012, pp. 1-10.N Trajcevski, M Kuzinovski, P Cichosz, Investigation of Temperature During Machining Process by High Speed Turning, *A tutorial review: 10th International Scientific Conference on Flexible Technologies*, 12 (1), 86-103, 2009.
8. H. Hashempour, F.J. Meyer and F. Lombardi, "Analysis and evaluation of multisite testing for VLSI", *IEEE Transactions on Instrumentation and Measurement*, Vol. 54, No. 5, pp. 1770-1778, October 2005.
9. D. R. Maria, K. Viswanathan, M. Amal and K. K. Kumar, "Automation of ATE test program execution in offline and online," 2017 IEEE 19th Electronics Packaging Technology Conference (EPTC), Singapore, 2017, pp. 1-5.
10. William J. Headrick and Gilberto Garcia, "Automated configuration of modern ATE", IEEE Instrumentation & Measurement Magazine, Vol. 21, No.4, pp. 22-26, August 2018.