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Implementation of 256 bit SRAM by using 45nm and 90nm technologies in Microwind

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Abstract - *In today's electronics world the most important need is to store maximum data in minimum space. The goal of proposed work is to design a memory having standard values of the parameters like power dissipation, leakage current, static noise margin, threshold voltage and gate oxide in small chip size with high memory read and writes speed. Our focus is to design a 256Bit memory in 45nm and 90nm technology using "Microwind". We are designing 256bit memory using combination of 256 1bit (1bit is equal to 6T SRAM cell, "T" stands for transistor) memory cell. Here 256bit consists of 256*6=1536 transistors. Microwind is a CMOS circuit editor and simulation tool for layout level design running on Microsoft window. It also allows us to draw the mask of circuit layout and perform analog simulation. This paper represents the simulation of 256bit SRAM memory using a low power reduction technique and their comparative analysis on different parameters.*

Key Words: SRAM, Microwind, CMOS, Power dissipation, leakage current, static noise margin, gate oxide thickness.

1. INTRODUCTION

Data storage devices are primarily used to store the data either temporarily or permanently depending on the. Application From the beginning of the electronics industry, storage of data has been a major point of consideration. Many storage devices have been developed by now, with various working principles and data storage techniques. Data storage devices can be classified by a wide variety of aspects but most frequently they are divided by technology into the semiconductor types and the moving media types. Memories are circuits or systems that store the information in large quantity, hence are vital components in modern integrated circuits. Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path toward both denser and faster integration. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20 years ago. As the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. Domination of digital VLSI designs, on chip memory is more essential. Mostly, SRAM is used as a cache memory in modern SoCs and it is used SRAM memory is used in a lot of devices where speed is more crucial than capacity. Here SRAM implemented through deep submicron CMOS technology because of its low static power consumption fast switching and its noise immunity.

2. SRAM ARCHITECTURE

SRAM architecture is drawn below. It consists memory cell array, write driver and pre- charge circuit, raw and column decoder, sense amplifier, data lines-data in and out.

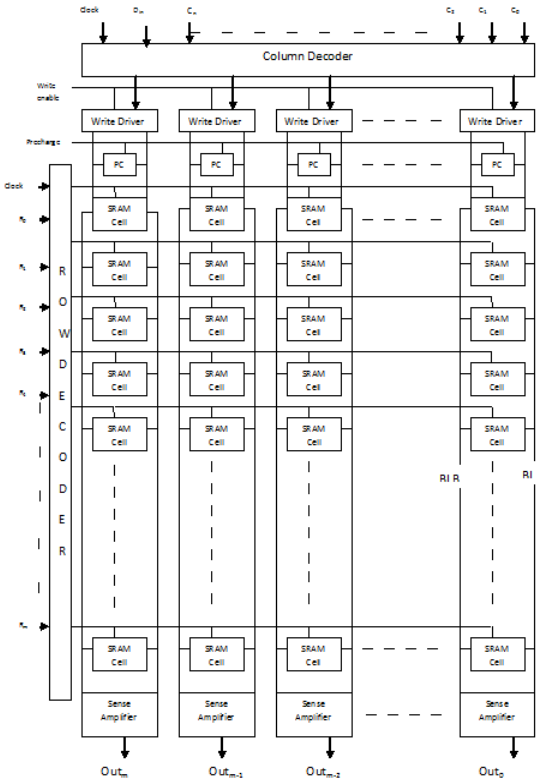

Fig2: detailed SRAM Architecture

If number of address lines are m and numbers of data lines are n, then total size of memory can be obtained as 2m+n.where popular numbers of m and n are 8, 16, 32, 64, 256 etc. In this architecture, rows denote word lines which indicate for selecting particular memory cell and column denote bit and bit-bar lines for inserting and retrieving data from it. Separate write driver and sense amplifier are dedicated to each column for fast read and write operation. This architecture possesses fast write and read operation due to its differential writing and sensing scheme.

2.1 Memory Cell

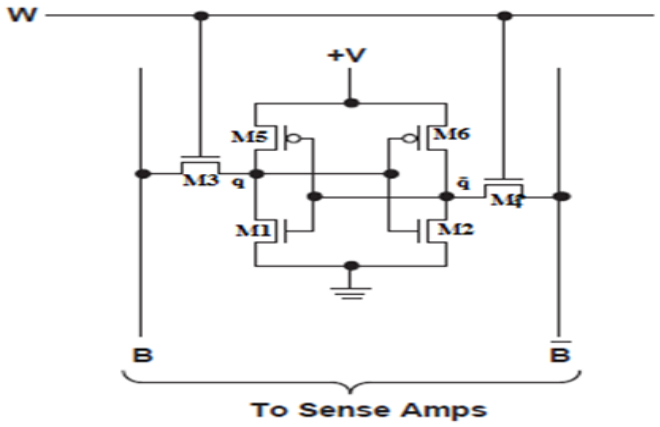

Fig2.1: 6T SRAM cell

6T SRAM cell each bit in an SRAM is stored on four transistors that form the two cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit. Access to the cell is enabled by the word line which controls the two access transistors M3 and M4 which in turn control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations.

The memory cell consists of a simple CMOS latch in which two inverters connected back to back and two complementary access transistors M1 and M2. The cell will preserve one of its two possible states, as long as the power supply is available.

A coupled inverter latch s popular in low power designs due to negligible static power consumption. Typically, this type of sense amplifier detects a voltage difference of one tenth of the VDD.

2.2 Sense amplifier

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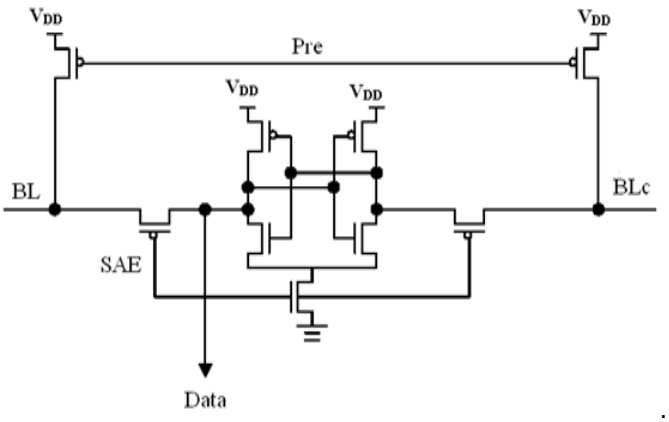

Fig2.2: Sense amplifier

3. SRAM Operation

Mainly, RAM operations are synchronized with its peripherals and given as data write, read and hold.

1. HOLD

2. READ

3. WRITE

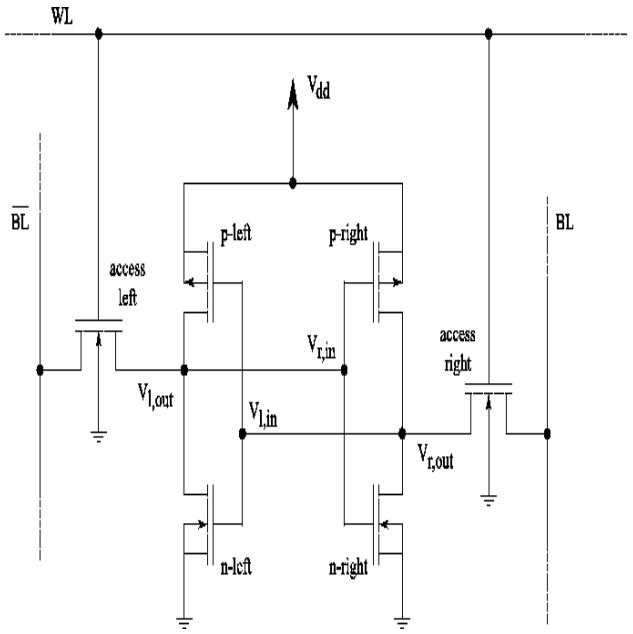

Fig3: Circuit of a 6 transistor SRAM cell. It consists of two CMOS inverters and two access MOSFETs

Hold state

When WL="0", M1 and M2 disconnect the cell from bit lines (Bit and bit bar). The current drawn in this state from the Vdd is termed as leakage current.

Read state

Read operations starts with pre-charging Bit and Bit bar to high. Within the memory cell M3 and M6 are ON. Asserting the world line, turns ON the M1 and M2 and the values of Q and Q' are transferred to bit-lines. No current flows through M2, thus M2 and M6 pull Bit bar up to Vdd, i.e., Bit="1" and Bit line discharges through M1 and M3. This voltage .difference is sensed and amplified to logic levels by sense amplifiers.

Write state

The value to be written is applied to the bit lines and keep WL="1". Thus to write data "0", we assert Bit=0, Bit bar="1", the Bit ="1", Bit bar="0".

4. Methodology

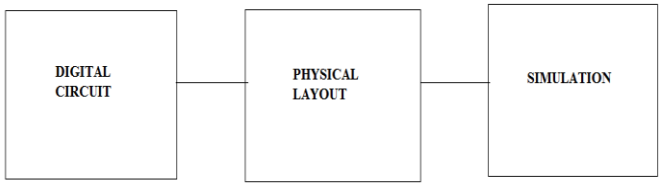

Fig4: Basic flow diagram of Microwind

4.1 Design flow using Microwind

MICROWIND supports entire front-end to back-end design flow. For front-end designing, we have DSCH (digital schematic editor) which posses in-built pattern based simulator for digital circuits. User can also build analog circuits and convert them into SPICE files and use 3rd party simulators like Win Spice or SPICE.

The back-end design of circuits is supported by MICROWIND. User can design digital circuits and compile here using Verilog file. MICROWIND automatically generates a error free CMOS layout. Although this place-route is not optimized enough as we do not indulge in complex place & route algorithms.

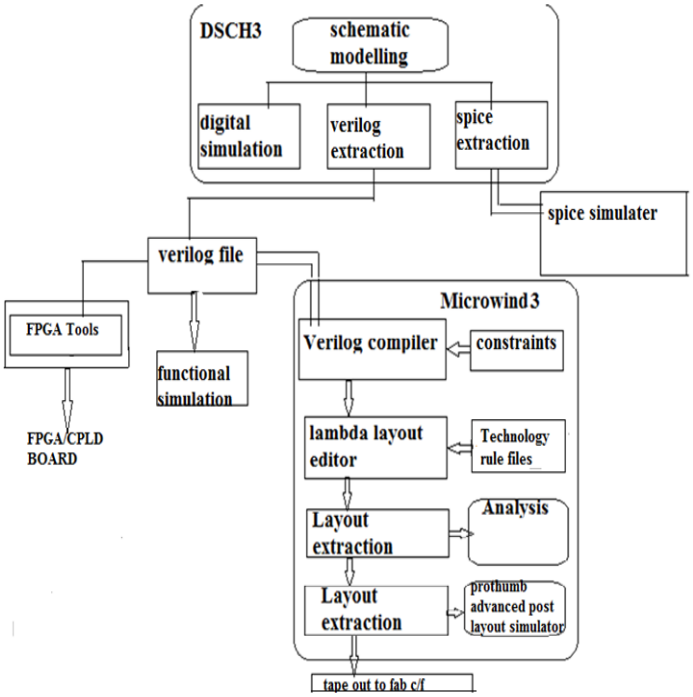

Fig4.1: Design flow using Microwind

4.3 Implementation of 256Bit SRAM

This gives the detailed implementation of SRAM, The circuitry involved in designing the SRAM and the operation of each block in the design.

The block diagram of the SRAM chip is shown in figure. The core memory is arranged in an 8*4 array of 6 transistor SRAM cells. The square layout is efficient in terms of silicon area.

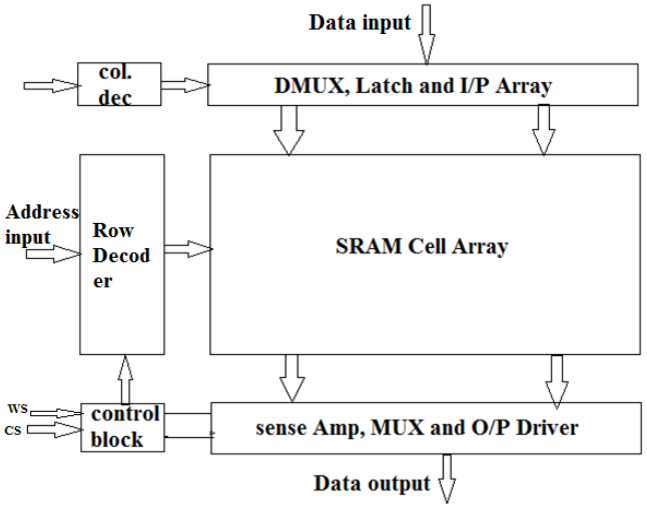

Fig 4.3: Block diagram of SRAM

5. Results

In the results, schematic level file implemented with high performance CMOS model for 90nm and customized

PTM CMOS model and layout of 1 bit memory in 45nm and 90nm has performed on Microwind.

5.1 layout design

The 1bit cell consists of 4 NMOS,2 PMOS. It consists of bit line, bit line bar and a word line. The 6T SRAM cell shown in the figure has two outputs BL and BLC and one input WL.BL is real value and BLC is the complementary value.

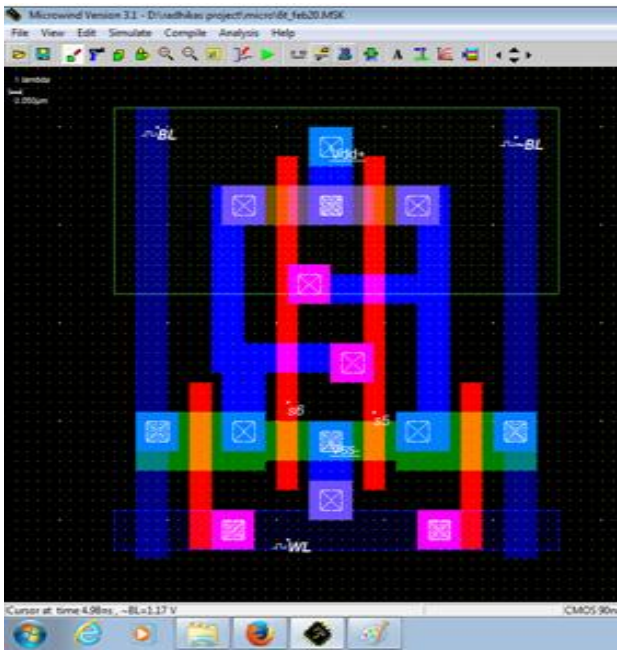

Fig 5.1: layout of 6T SRAM cell in 90nm Technology

5.1.1: layout of 6T SRAM cell in 90nm Technology

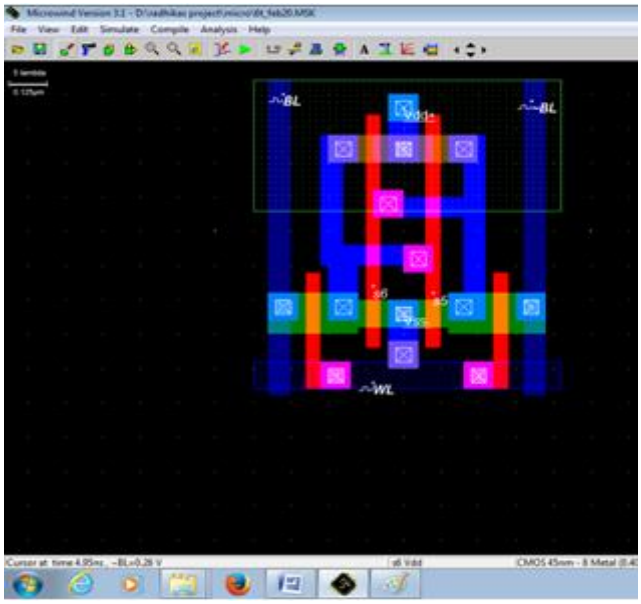

Fig 5.1.1: layout of 6T SRAM cell in 90nm Technology

5.1.2 Layout of 6T SRAM cell in 90nm Technology

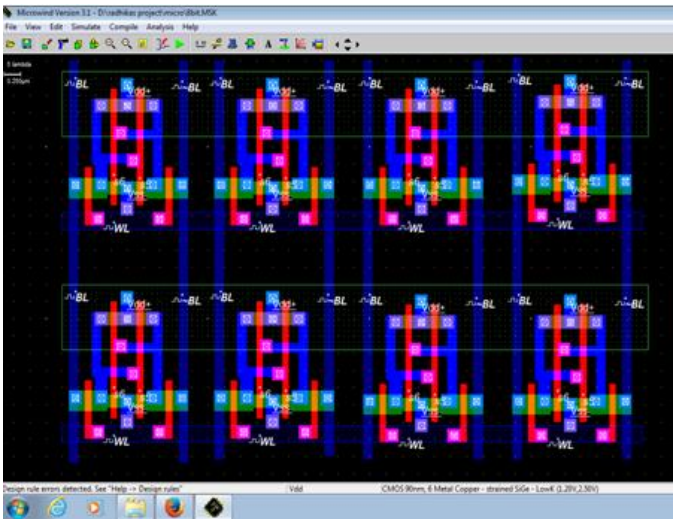

Fig 5.1.2: layout of 6T SRAM cell in 90nm Technology

5.1.3 Layout of 6T SRAM cell in 90nm Technology

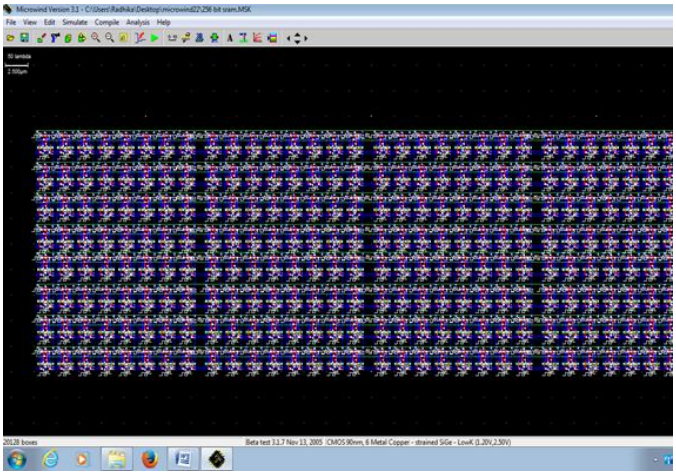

Fig 5.1.3: layout of 6T SRAM cell in 90nm Technology

5.2 Output Waveforms

The 1bit cell consists of 4 NMOS, 2 PMOS. It consists of bit line, bit line bar and a word line. The 6T SRAM cell shown in the figure has two outputs BL and BLC and one input WL.BL is real value and BLC is the complementary value. The layout is having six transistors and two metal lines lead the outputs. The data and ~data signals similar to BL and ~BL in the schematic Word line are the WL signal.

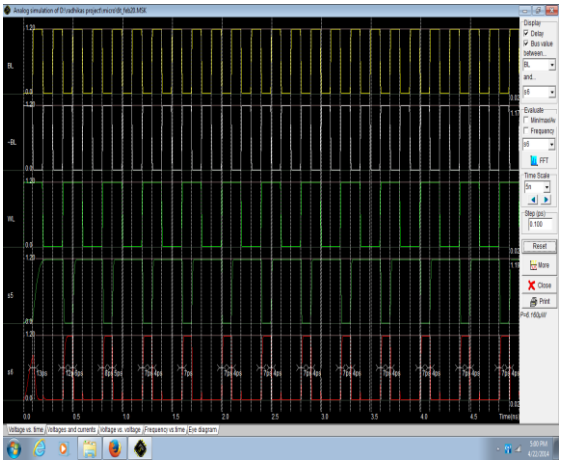

Fig5.2: Simulation output of 6T SRAM cell

5.2.1 Simulation output of 6T SRAM cell by using 45nm technology

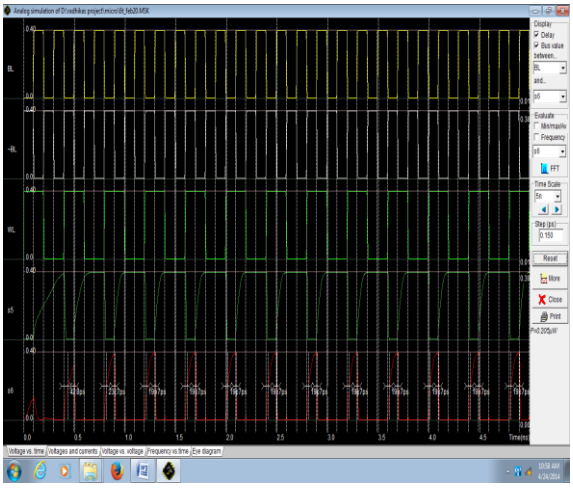

Fig 5.2.1: simulation output of 6T SRAM using 45nm technology

5.2.2 Simulation output of 8bit SRAM in Microwind

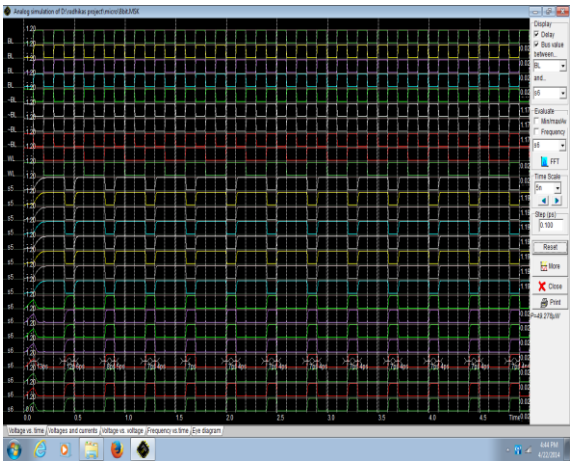

Fig5.2.2: Simulation output of 8bit SRAM

5.2.3 Simulation output of 256bit SRAM using Microwind in 90nm technology

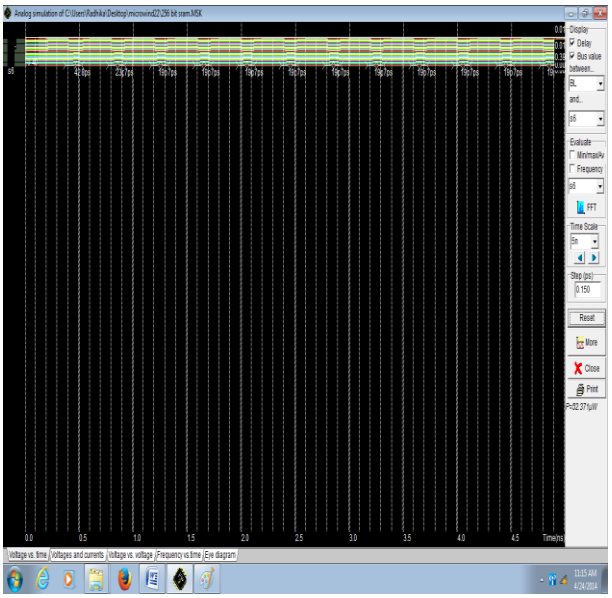

Fig 5.2.3: Simulation output of 256 bit SRAM

6. COMPARATIVE ANALYSES

Comparisons of read delay and write delay, power dissipation between 6T, 8T SRAM Cell

The simulation results of 8T SRAM cell are analyzed and compared with the conventional 6T SRAM cell for cell ratio, pull up ratio, data retention voltage, read margin, write margin, threshold variations and temperature variations

Table6: Comparison of read delay and write delay, power dissipation between 6T, 8T, 9T SRAM Cell

SRAM Cell	READ DELAY (ps)	WRITE DELAY (ps)	POWER DISSIPATION
6T	80	9	51.7
8T	11	65	101

After comparing the 6T and 8T SRAM cell, it is found that 6T SRAM cell provide a very low write delay nearly 7 times lesser when compared to 8T SRAM cell. While in case of read delay there is less difference, read delay of 8T SRAM is nearly 1.35 times higher as compared of to 6T SRAM. The power dissipation of 6T SRAM is half of power dissipated in 8T sram. This is due to more number of transistor in 8T SRAM and secondly little complex working than other one

6.1 Read margin Vs pull up ratio

Table presents the read margin of 8T SRAM cell calculated by varying the cell ratio and comparison with 6T is also done. Read margin of 8T SRAM cell is directly

proportional to cell ratio i.e read margin increases when cell ratio increases.

Table 6.1: Read margin Vs Cell ratio

CR	Read margin (mv) 8T cell	Read Margin (mv) 6T cell
0.8	0.449	0.194
1.0	0.455	0.196
1.2	0.461	0.200

6.2 Write margin Vs pull up ratio

Table presents the write margin of 8T SRAM cell calculated by varying the pull up ratio and comparison with 6T is also shown. Write margin of 8T SRAM cell is directly proportional to pull up ratio i.e write margin increases when pull up ratio increases.

Table 6.2: Write margin Vs Pull up Ratio

PR	Write margin (mv) 8T cell	Write margin (mv)
3.0	0.50	1.246
3.2	0.52	0.249
3.4	0.55	0.253

7. CONCLUSIONS

The stability performances of three SRAM cell topologies have presented. As process technologies continue to advance, the speed of SRAMs will increases, but devices will be more susceptible to mismatches, which worsen the static-noise margin of SRAM cell. The 6T SRAM provide very less RNM. To obtain higher RNM in 6T SRAM cell width of the pull down transistor has to be increased but this increases area of the SRAM which in turn increases the leakage currents. Analog simulation results in standard 0.70um CMOS technology shows the layout of 6T SRAM cell has correct read/write operation. Hence SRAM is designed and implemented at the layout level using MICROWIND tool.

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