International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 6 | June 2020 www.irjet.net p-ISSN: 2395-0072

A study of HVDC Circuit Breakers and Matlab/Simulink based designing of Multi pole HVDC Test-Bed

Jamaludin[1], M.K.Bhasakr[2], Manish Parihar[3] and Surendra Singh[4]

[1]ME Scholar, [2]Professor, [3&4]PhD Scholar,
Department of Electrical Engg., MBM Engineering College, Jai Narayan Vyas University, Jodhpur, India

---

Abstract - *High Voltage Direct Current (HVDC) power transmission has gained serious popularity in last 6 decades, suggesting a valid alternative to the currently, almost exclusively used, AC power transmission. New innovations in converter technology made HVDC an even more promising solution on energy distribution and transmission. The use of high voltage direct current (HVDC) circuit breakers (CBs) with the capabilities of bidirectional fault interruption, reclosing, and re-breaking can improve the reliable and safe operation of HVDC grids. There are still a number of problems in the technology if we want to talk about DC Circuit Breakers. The main issue is the interruption of the short circuit current in order for the line to shut down when a problem occurs on the grid. DC breakers are the key factor for the accomplishment of a function DC grid. Voltage source converter based HVDC (VSC-HVDC) system is the best option for realizing future multi-terminal HVDC system to integrate bulk amount of energy over long distances to the AC grid. Recently, studies on HVDC circuit breaker (CB) prototypes have shown successful take a look at results. DC current breaking topologies on ways of achieving artificial zero should be somewhat modified. As another, one possible resolution is to mix fault current limiting technologies with dc breaking topologies. We have presented simulation and analysis about application of resistive Superconducting Fault Current Limiters (SFCLs) on Hybrid HVDC CB so as to estimate the consequences of combining fault current limiters and conventional dc breakers.*

***Key Words*: SFCL, HVDC Circuit Breaker, VSC-HVDC, , Hybrid HVDC CB, HVDC Grids.**

1. INTRODUCTION

Circuit breakers are fundamental elements for a safe and code-compliant electrical installation. Conductors and electrical equipment are exposed to damage and malfunction, and there is always a risk that someone may connect a device incorrectly or use it for the wrong application. These conditions can cause a device to draw current above its rated value, and the corresponding circuit breaker trips to disconnect the fault. Before providing an overview of circuit breakers, it is important to understand the difference between the two main current conditions that cause a circuit breaker to trip. The HVDC circuit breaker is a switching device that interrupts the flow of abnormal direct current in the circuit. When the fault occurs in the system, the mechanical contacts of the circuit breaker are pulled apart and thus their circuit is open. In HVDC circuit breaker, circuit breaking is difficult because the current flow through it is unidirectional and there is no zero current. Circuit breakers will be positioned on DC grids and act when a fault occurs. Breakers would have to fulfill some basic requirements. Current zero crossing should be created to interrupt the current once a fault occurs [1].

order to achieve commercial application of future Multi Terminal HVDC (MTDC) networks, typically considered an optimum solution for renewable energy transmission and power grid inter-connection, the reliability of HVDC systems must be guaranteed [2], [3]. Conventional point-to-point HVDC systems can be sufficiently protected via mechanical circuit breakers located on the AC side [4]; however, a selective coordination protection scheme that isolates faulted lines should be utilized in MTDC to prevent the blackout of the entire grid system [5]. HVDC circuit breakers (HVDC CB) are widely considered a key technology in the implementation of the MTDC system [6].

Generally, fault current interruption can be easily achieved via zero-current crossing. While AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption. To fulfill the zero-crossing condition of DC fault current, a forced current reduction method should be utilized, and various type of HVDC CB are summarized in [7], some of which have revealed prototypes and successful test results. Nevertheless, an effective and reliable solution considering massive fault energy during DC fault interruption is still lacking. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat modified [8]. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies. In this work, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers.

Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [8]. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and

improving the performance of HVDC CBs. In order to estimate the performance of combined application of SFCL on HVDC CBs, simulation studies were performed using Matlab/Simulink.

2. Modeling of SFCL and HVDC Circuit Breaker

Hybrid HVDC circuit breaker and SFCL were modeled, and fault current interruption characteristics were obtained to determine the Hybrid HVDC CB suitability for the application of SFCL considering the current interruption capability and reduction of total dissipated energy during DC fault.

2.1 HVDC Test-bed Model

In order to analyze the impact of SFCL on various types of HVDC CBs, a test-bed model was designed in Matlab /Simulink as illustrated in Fig.1 The simple, symmetrical, monopole, point-to-point, 2-level, half-bridge HVDC system was utilized to concentrate the interruption performance of the DC fault current in detail. The AC network adjacent to the HVDC link was substituted by equivalent RL impedance, which enabled the X/R ratio of the power system to be determined.

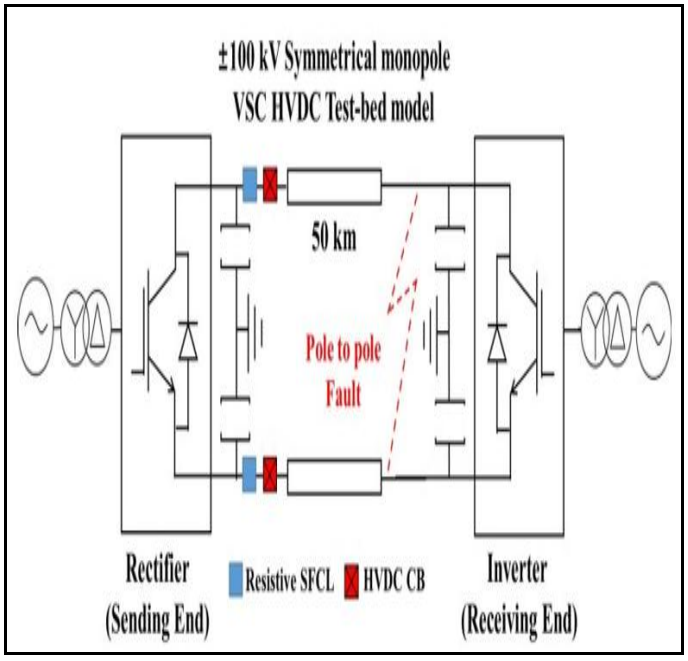

Fig -1: level point-to-point HVDC test-bed model (V_{ac}: AC voltage, R_{ac}, Lac: system impedance of AC, L_p: Phase reactor)

The converter transformer was a wye-delta connection. A phase reactor, L_p, was added between the converter and transformer to filter the harmonics during conversion. Each type of HVDC CB and SFCL was located at the output of the rectifier. Detailed specifications of the HVDC link are as follows: the rated voltage = ±100 kV, nominal current = 1 kA, nominal power flow = 100 MW, and the transmission line length = 50 km.

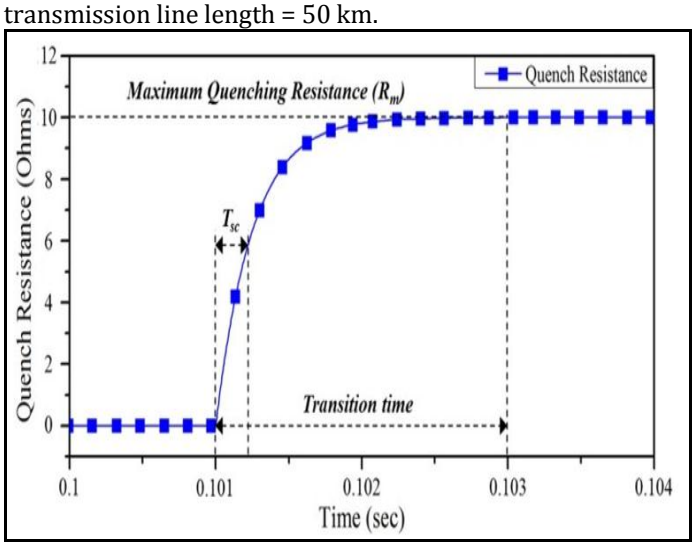

Fig -2: Quenching characteristics of the designed resistive SFCL with time.

2.2 Resistive Superconducting Fault Current Limiter

The resistive SFCL, which is based on the quenching phenomena of superconductors, has been an area of great interest for researchers in the last decade [10], and several prototypes have been developed and installed in medium- and high-voltage systems [11]. Focusing on the theoretical approaches for a resistive SFCL [12],the quenching phenomena of SFCL can be expressed as:

$$R_{SFCL}(t) = \begin{cases} 0 & (t < t_{quenching}) \\ R_m(1-\exp(-t/T_{sc})) & (t_{quenching} < t) \end{cases}$$

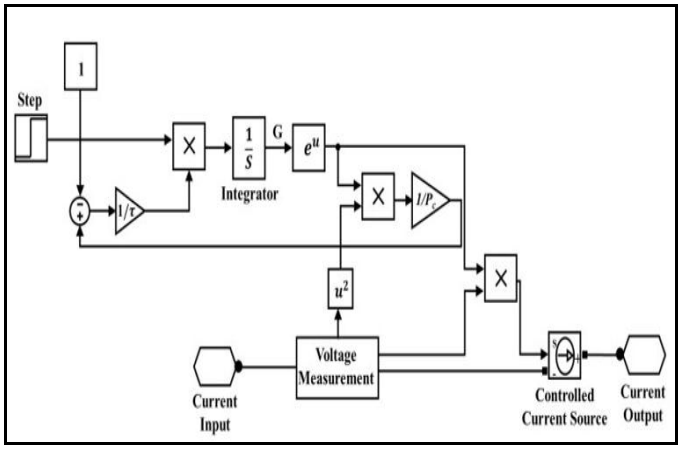

Fig -3: The modified Mayr black-box arc model designed using Matlab/ Simulink for discrete simulation environment

Where R_m is the maximum quenching resistance and TSC is the time constant for the transition to the quenching state. In this work, the SFCL rating was 100 kV DC with a 2 kA of critical current. The maximum quenching resistance, R_m, is 10 Ω. In order to acquire nearly 10 ohms of R_q within 2 ms, the value of T_{sc} was determined to 0.25 ms. the quenching characteristics of the designed SFCL based on above equation are shown in Fig. 2.

3. Case study

Transient fault simulations were conducted to analyze the effects of SFCL on various HVDC CB types. Each type of HVDC CB, both with and without SFCLs, was applied at the sending end of the test-bed.

The representative HVDC CB topologies are categorized as follows: mechanical CB (MCB), passive resonance CB (PRCB), inverse current injection CB (I-CB) and Hybrid DC CB (HDCCB).The concepts of HVDC CB are classified in CIGRE WG. B4.52, according to the method to achieve artificial current zero to interrupt fault current [16].

3.1 Mechanical CB (MCB)

This concept has been used for low-voltage DC breakers of few kilovolts only, which is usually in air-blast CB or SF6 CB [19]. In case of MCB, a DC current is reduced by increasing the arc voltage to higher value than that of the system voltage. By utilizing the designed black-box arc model, the simulation model of MCB was designed as shown in Fig. 4(a). In order to achieve the practical approach of simulation results, the delay time was assumed as 10 ms.

3.2 Passive resonance CB (PRCB)

To dissipate the energy stress on the MCB, the secondary path with a series L-C circuit is added as shown in Fig. 4(b). When the fault occurred at 0.1 sec, MCB opens with 10 ms of delay considering opening delay, and then an arc forms across the contacts with increasing arc impedance. The DC current begins to commutate and resonate in the secondary path after the arc impedance exceeds the L-C impedance. When a DC current of the primary path meets zero crossing, a current through the MCB can be interrupted by the extinction of the arc. An additional parallel surge arrester (SA) circuit is supplemented to prevent voltage stress across the PRCB during arc extinction.

3.3 Inverse current injection CB (I-CB)

This scheme is similar to PRCB. However, the pre-charged capacitor via an additional DC power source injects an inverse current into the primary path after the current commutates to secondary path as shown in Fig. 4(c). This can reduce the interruption and oscillation time when compared to that of PRCB. Before a fault, a charging switch (ACB1) and an auxiliary switch (ACB2) maintains closed state. Thereby capacitor can be charged by DC source. When a fault occurs, after an 10 ms delay, MCB and ACB1 contacts open simultaneously. Then the high discharging inverse current from capacitor is supplied to main path. The fault current is rapidly decreased and transient recovery voltage appears between the terminals of ICB.

When the voltage exceeds to the knee voltage of SA, it is triggered to restrain the voltage rise, and it absorbs the fault energy. After 3 ms from the time when MCB and ACB1 were opened, ACB2 is triggered and it isolates the secondary path. This opening of ACB2 will prevent the current to flow through the secondary path which could make additional LC resonance current. Therefore, remaining fault energy is exclusively absorbed by SA. If the current reaches to zero, a residual circuit breaker (RCB) opens and the current interruption is complete.

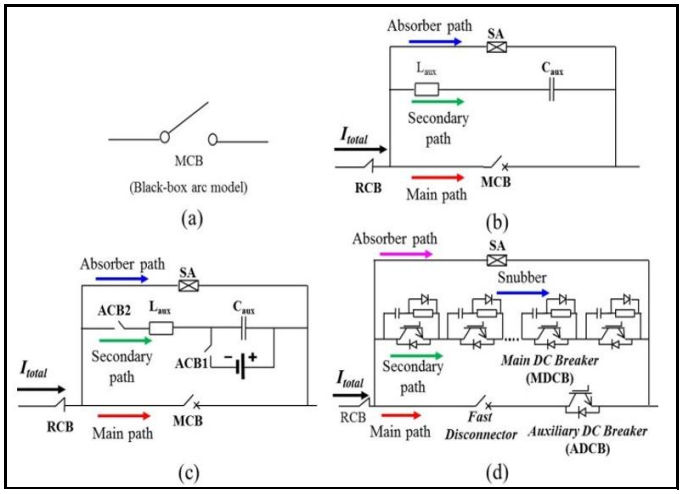

Fig -4: HVDC CB models: the (a) Mechanical CB (MCB), (b) Passive resonance CB (PRCB), (c) Inverse current injection CB (I-CB), and (d) Hybrid DC CB (HDCCB).

3.4 Hybrid DC CB (H-DCCB)

This scheme is widely considered as the optimal concept for interrupting DC fault current, was designed as illustrated in Fig. 4(d) [21]. The delay times of IGBT was assumed as Δt_{IGBT} = 6 μs in simulation. When a DC fault occurs, the auxiliary DC breakers (ADCB) and fast dis-connector are opened sequentially, then the current starts to commutate from the main path to secondary path. After commutation, main DC circuit breakers (MDCB) in secondary path are opened, and total current is reduced because the current flows to the snubber circuit of MDCB until the parallel-connected SA trips. When the voltage across the HDCCB terminals exceed to knee voltage, the SA ignites and forces the DC fault current to zero by absorbing remaining fault energy. Finally, a RCB opens and isolates the DC fault.

Except for the non-arc type such as inverse current injection and Hybrid DC CB, the implementation of arc dynamics is a major concern in the design for an accurate simulation model. The black-box arc model, which represents the arc dynamics by calculating the differential equation of the arc conductance, was designed. The simulation models of HVDC CBs is given as under-

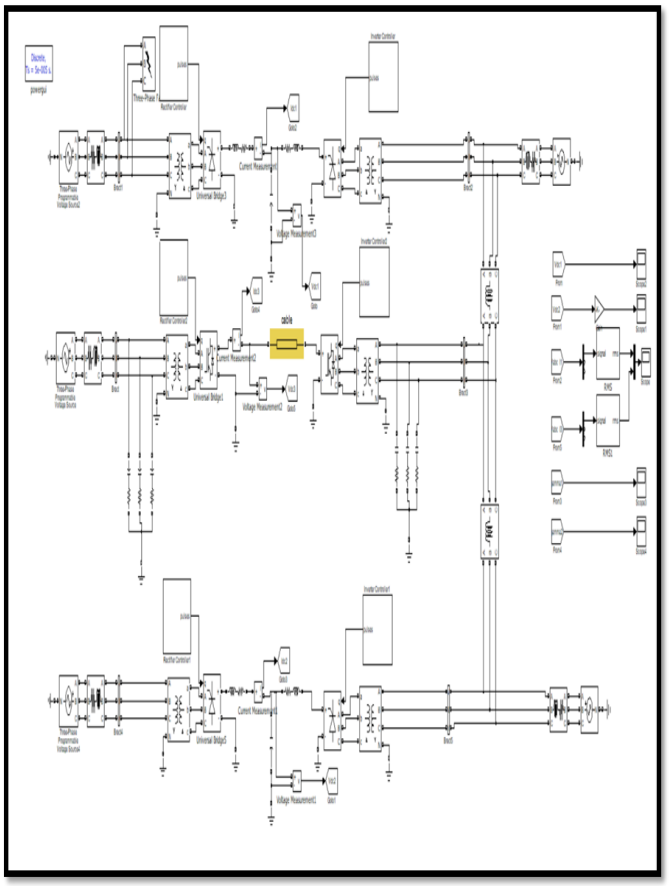

Fig -5: Proposed System for Multi-pole HVDC

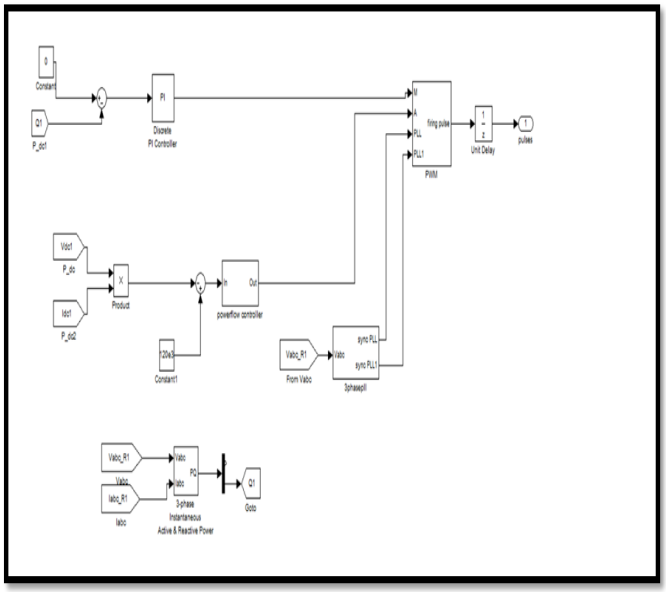

Fig -6**:** Controlling subsystem

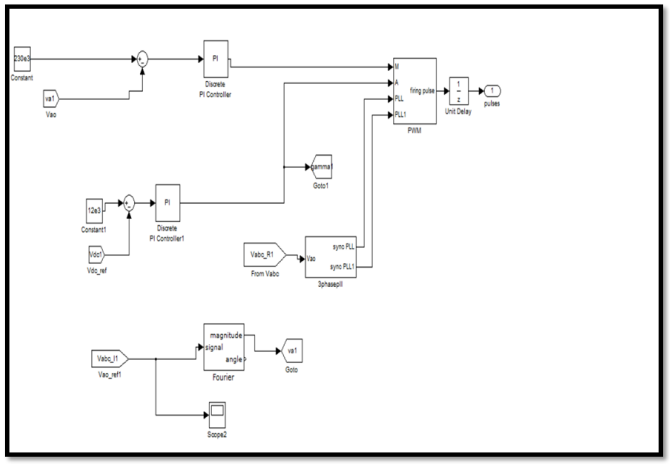

Fig -7: Inverter control subsystem

In this work, we investigated application studies of resistive SFCL on the Multi Pole HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [9]. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs.

In order to estimate the performance of combined-application of SFCL on HVDC CBs, simulation studies were performed using Matlab/Simulink. Four types of DC breakers and SFCL were modeled, and fault current interruption characteristics were compared to determine the HVDC CBs type most suitable for the application of SFCL considering the

current interruption capability and reduction of total dissipated energy during DC fault.

4. Simulation Results

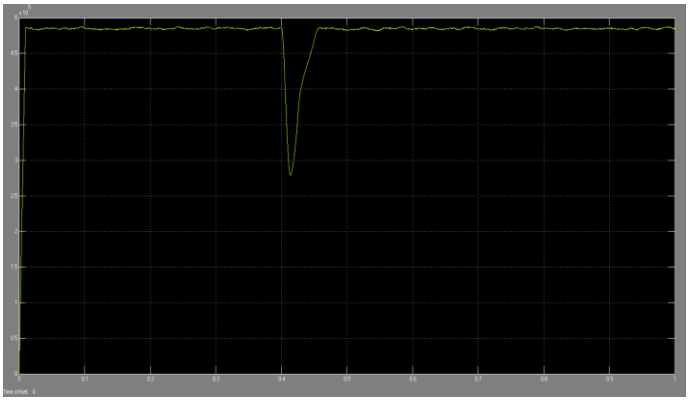

Fig -8: Vdc-1 Variation

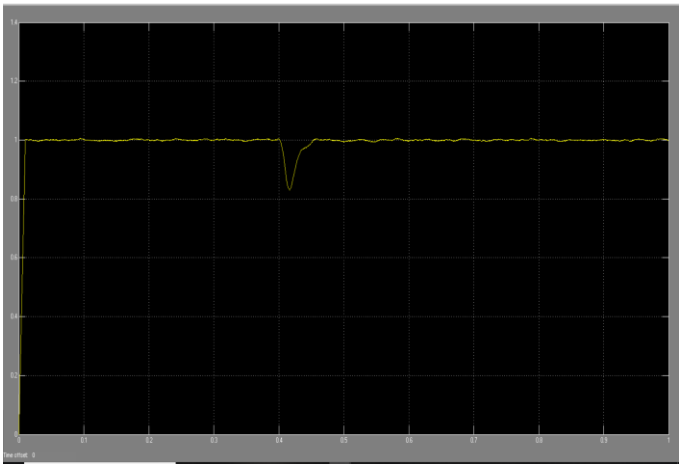

Fig -9: Vdc-2 Variation

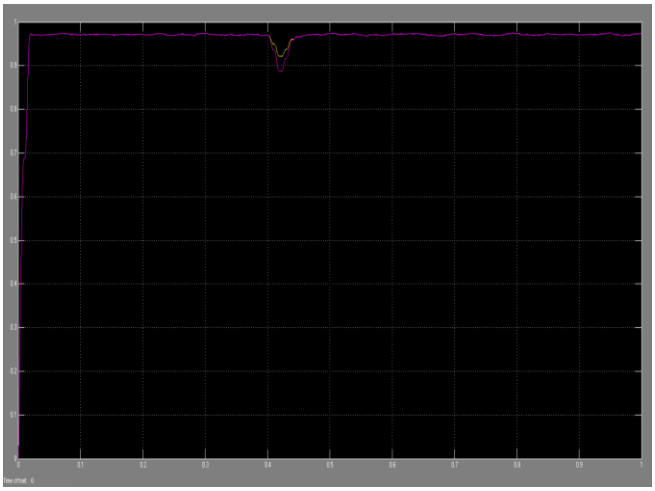

Fig -10: Current Variation

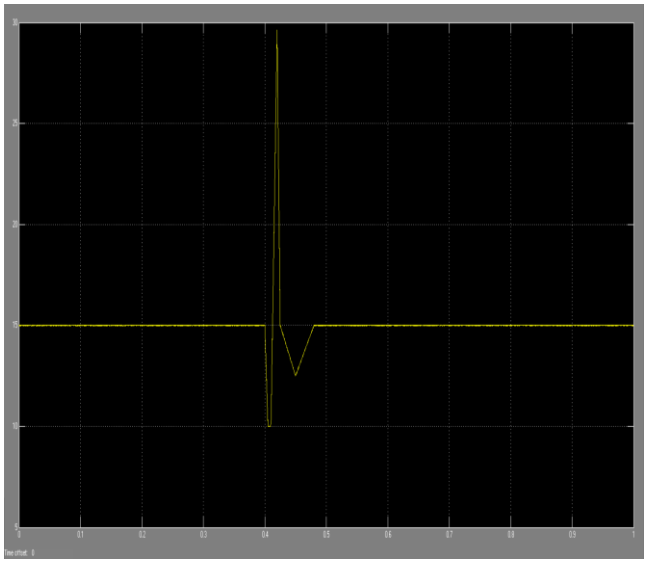

Fig -11: Tripping of CB1

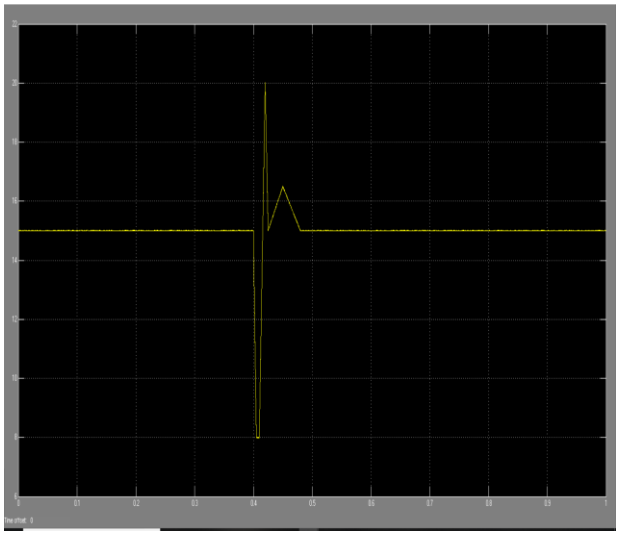

Fig -12: Tripping of CB2

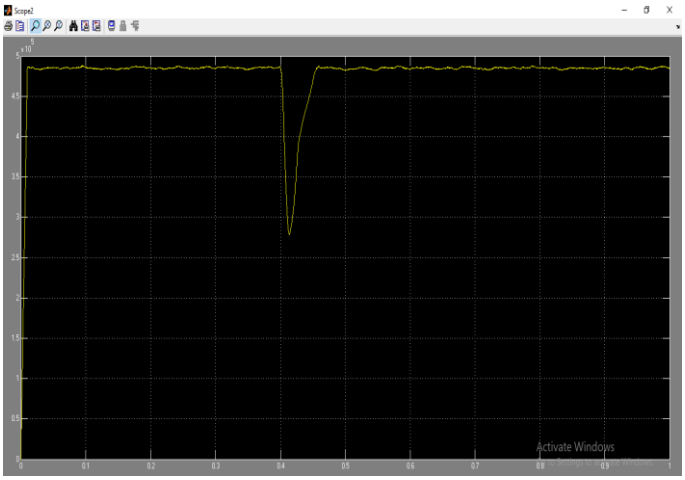

Fig -13: Voltage Variation for Multi Pole HVDC

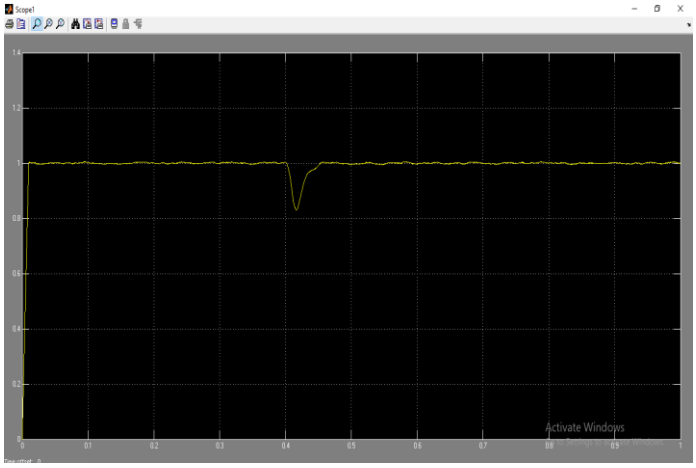

Fig -14: Current Variation for Multi Pole HVDC

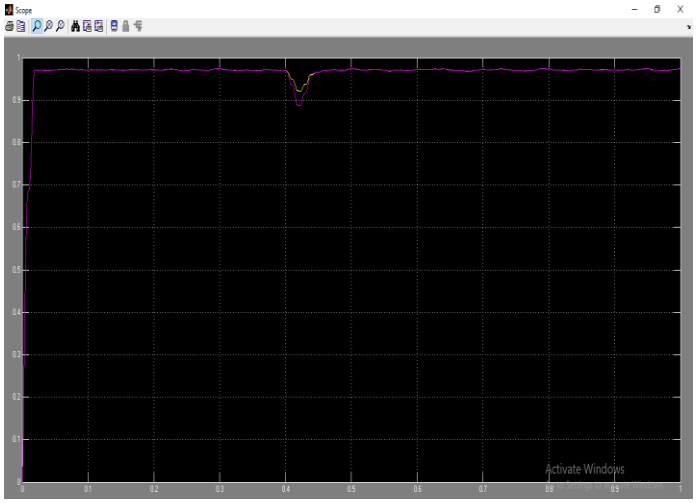

Fig -15: Sending and Receiving end Current Variation

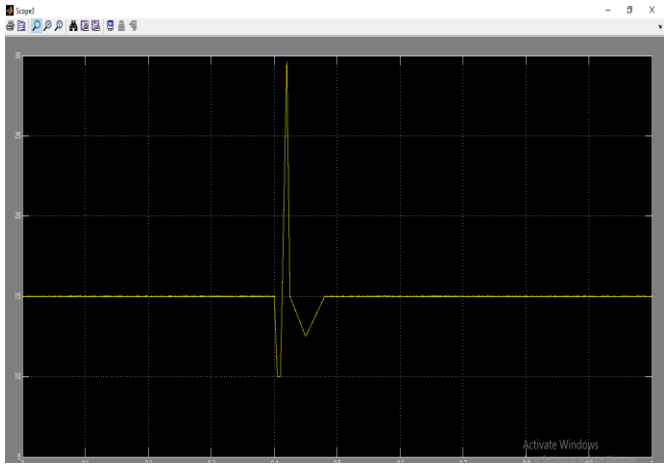

Fig-16: Trip CB-1

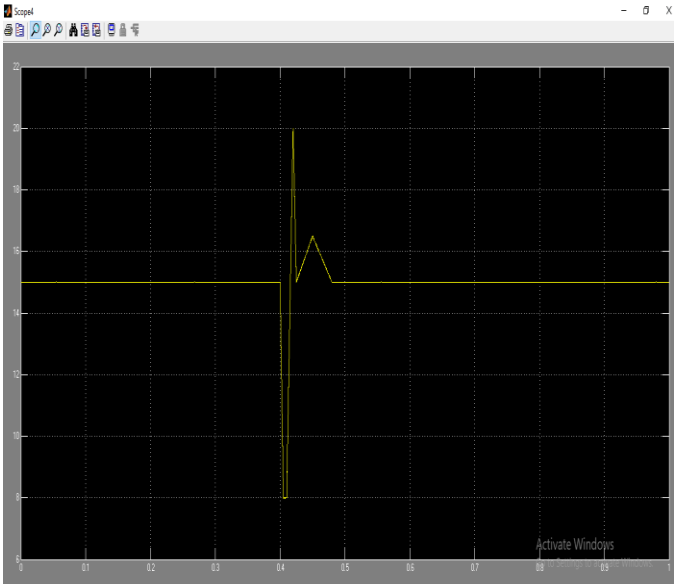

Fig-17: Trip CB2

5. Conclusion

This research paper deals with the impact of SFCL on various types of HVDC CB. The resistive SFCL considers quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC test-bed were designed using Matlab/Simulink. A severe DC multi pole fault was imposed to analyze the interruption performance. From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL.

REFERENCES

[1] Ataollah Mokhberdoran, Adriano Carvalho, Helder Leite and Nuno Silva, "A Review on HVDC Circuit Breakers," IET Renewable Power Generation Conference, September 2014.

[2] Jong-Geon Lee, Umer Amir Khan, Ho-Yun Lee and Bang-Wook Lee, "Impact of SFCL on the Four Types of HVDC Circuit Breakers by Simulation", 2015 IEEE.

[3] H. Y. Lee, A. Mansoor, K. H. Park and B. W. Lee, "Feasible Application Study of Several Types of Su-perconducting Fault Current Limiters in HVDC Grids", 1051-8223 (c) 2018.

[4] W R Leon Garcia, A Bertinato, P Tixador , B Raison , B Luscan, "Full-selective protection strategy for MTDC grids based on R-type superconducting FCLs and mechanical DC circuit breakers", IEEE 2017.

[5] Umer Amir Khan, Jong-Geon Lee, Faisal Amir and Bang-Wook Lee, "A Novel Model of HVDC Hybrid-Type Superconducting Circuit Breaker and Its Performance Analysis for LimitingAnd Breaking DC Fault Currents", IEEE Transactions On Applied Superconductivity, VOL. 25, NO. 6, Dec. 2015.

[6] G. Saldaña, et al , "Impact of a Resistive Superconductive Fault Current Limiter in a Multi-Terminal HVDC Grid", 978-1-5386-3738-8/18/$31.00 ©2018 IEEE.

[7] Lei Gao, Bin Xiang, Kun Yang, Zhiyuan Liu, Yingsan Geng, Satoru Yanabu, "The Comparison of DC Semiconductor Circuit Breaker and SF6 Circuit Breaker with Transverse Magnetic Field for DC Transmission", IEEE 2017.

[8] W. Leon Garcia, P. Tixador, B. Raison, A. Bertinato, B. Luscan and C. Creusot, "Technical and Economic Analysis of the R-type SFCL for HVDC Grids Protection", 1051-8223 (c) 2017 IEEE.

[9] Steven M. Blair et al., "Analysis of energy dissipation in resistive superconducting fault current limiters for optimal power system performance," IEEE Trans. Appl. Supercond., vol. 21, no 4, pp. 3452- 3457, Aug. 2011.

[10] Umer Amir Khan, et al., "A novel model of HVDC hybrid-type superconducting circuit breaker and its performance analysis for limiting and breaking DC fault current," IEEE Trans. Appl. Supercond., vol. 25, no. 6, Dec. 2015, Art. ID. 5603009.

[11] H. Kim et al., "Development and grid operation of superconducting fault current limiters in KEPCO," IEEE Trans. Appl. Supercond., vol. 24, no. 5, Oct. 2014, Art. ID. 5602504.

[12] H. J. Lee et al., "Effect of a SFCL on commutation failure in a HVDC system," IEEE Trans. Appl. Supercond., vol. 23, no 3, Jun. 2013, Art. ID. 5600104.

[13] M. Noe and M. Steurer, "High-temperature superconductor fault current limiters: Concepts, applications, and development status," Supercond. Sci. Technol., vol. 20, no. 3, pp. R15-R29, Jan. 2007.

[14] Y. Shiraiet al., "Simulation study on operating characteristics of superconducting fault current limiter in one-machine infinite bus power system," IEEE Trans. Appl. Supercond., vol. 13, no. 2, pp. 1822–1827, Jun. 2003.

[15] Umer Amir Khan et al., "Feasibility analysis of the application and positioning of DC HTS FCL in a DC micro grid through modeling and simulation using Simulink and Simpowersystem," Phys. C, Supercond., vol. 471, no. 21-22, pp. 1322–1326, Nov. 2011.

[16] CIGRE Working Group B4.52 "HVDC grid feasibility study: appendix H", International Council for Large Electric Systems (CIGRE), Technical Brochure 533, Apr. 2013.

[17] O. Mayr, "Beiträgezurtheorie des statischen und des dynamischenlichtbogens," Arch. Elektrotech., vol. 37, no. 12, pp. 588–608, Dec. 1943.

[18] Pieter H. Schavemaker, Lou van der Sluis, "An improved Mayr-type arc model based on current-zero measurements", IEEE Trans. Power Del., Vol. 15, no. 2, pp. 580-584, Apr. 2000.

[19] M. Bucher, C. M. Frank, "Fault current interruption in multiterminal HVDC networks," IEEE Trans. Power Del., vol. 31, no. 1, pp. 87-95, Feb. 2015.

[20] M. M. Walter, "Switching arcs in passive resonance HVDC circuit breakers," Ph.D. dissertation, ETH, Zurich, 2013. [Online]. Available: DOI: 10.3929/ethz-a-010112102.

[21] P. H. Shavemaker, et al., "The arc model blockset", in proc. The second IASTED international conference power and energy system (EuroPES), Crete, Jun. 2002.

[22] M. Callaviket al., "The Hybrid HVDC breaker," ABB Grid Systems, Technical paper, Nov. 2012.

[23] T. Harish, K. JithendraGowd, "SFCL with 5 – Level Inverter Using Four Types of HVDC Circuit Breakers", International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 3, Issue 6, pp.796-804, September-October-2017.

[24] S. Weniga,∗, M. Goertz a, M. Heinischa, S. Beckler b,∗, M. Kahl b, M. Suriyaha, T. Leibfrieda, J. Christianb a "Internal converter- and DC-fault handling for a single point grounded bipolar MMC-HVDC system" a-Karlsruhe Institute of Technology (KIT), Institute of Electric Energy Systems and High Voltage Technology (IEH), Karlsruhe BW 76131, Germany b -TransnetBW TSO, Stuttgart BW 70173, Germany Accepted 17 April 2018.

[25] M. Marz et al., "Mackinac HVDC converter automatic runback utilizing locally measured quantities", *Proc. CIGR*, pp. 22-24, Toronto, ON, Canada, Sep. 2014.

[26] J. Gerdes, "Siemens debuts HVDC PLUS with San Francisco's trans bay cable", *Living Energy*, vol. 5, pp. 28-31, Jul. 2011, [online] Available: http://www.energy.siemens.com/hq/pool/hq/energy-topics/living-energy/issue-5/LivingEnergy_05_hvdc.pdf.

[27] S Umashankar ; V. K. Arun Shankar ; Geet Jain ; Mohan L Kolhe "Comparative evaluation of pulse width modulation techniques on effective DC link voltage utilization of grid connected inverter" 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT).

[28] P. Tripura, Y.S. KishoreBabu, Y.R. Tagore, "space vector pulse width modulation schemes for two-level voltage source inverter", *ACEEE Int. J. on control system and instrumentation*, vol. 02, no. 03, October 2011.

[29] A V Bondarev1 , S V Fedorov1 , E A Muravyova2 ,1Kumertau branch of Orenburg State University, 2 Sovetsky Lane, 3b, Kumertau, Russia, Bashkortostan, 453300, 2Stelitamak branch of Ufa State Petroleum Technical University, 2, October Avenue, Sterlitamak, Russia, Bashkortostan, 453118 "Control Systems with Pulse Width Modulation in Matrix Converters" IOP Conf. Series: Materials Science and Engineering 327 (2018).

[30] Bondarev A V, Muravyova E A, Kadyrov R R, Rahman P A 2016 The analysis of opportunities of construction and use of avionic systems on base COTS-modules. ARPN Journal of Engineering and Applied Sciences .

[31] Tomasz Rudnicki, Andrzej Sikora, Robert Czerwinski, Tadeusz Glinka, (2018) "Impact of PWM control frequency on efficiency of drive with 1 kW permanent magnet synchronous motor", COMPEL - The international journal for computation and mathematics in electrical and electronic engineering, Vol. 37 Issue: 1, pp.307-318, https://doi.org/10.1108/COMPEL-01-2017-0031.

[32] Sanjib Kumar Nandi ; Ridown Rashid Riadh ; SiddikurRahman "Investigation of THD on a 12-pulse HVDC transmission network and mitigation of harmonic currents using passive filters" 2nd International Conference on Electrical Information and Communication Technologies (EICT), 2015.

[33] Dr. Ali NathemHamoodi et al ."Artificial Neural Network Controller for Reducing the Total Harmonic Distortion (THD) in HVDC". International Journal of Advanced

Engineering, Management and Science(ISSN: 2454-1311),vol 4, no. 1, 2018, pp.066-073 Infogain Publication, doi:10.22161/ijaems.4-1-11.

[34] RuchiAgarwal ; Sanjeev Singh "Harmonic mitigation in voltage source converters based HVDC system using 12-pulse AC-DC converters" Annual IEEE India Conference (INDICON), 2014.

[35] BanishreeMisra ; ByamakeshNayak "Understanding the control of 12-pulse thyristor converters in VSC-based HVDC system with passive filters" Technologies for Smart-City Energy Security and Power (ICSESP), Bhuwaneshwar,India,2018.