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FPGA based Control of DC-DC Converters for High Reliability Applications

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Abstract- *Switch mode DC-DC power converters are inherent to any electronic gadgets, motor drives and electric/ electronic systems. These power supply aim at providing a precise output voltage/current to the various components in a target. But usually the output of these converters need to be actively controlled using a closed loop control system for attaining output stability. Digital control is preferred over analog control since it has advantages of low power consumption, high noise margin, less component variation and programmability. There are different programmable digital devices like Microcontroller, Digital sign processor (DSP), Very Large-Scale Integrated Circuits (VLSI) for such applications. This venture centers around the FPGA based advanced digital control of high voltage dc-dc isolated dc-dc converter for high reliability satellite application.*

Key Words: FPGA, DC-DC converters, Hall thruster, Buck converter, Boost converter, VHDL, Pulse Width Modulation

1. INTRODUCTION

Space propulsion systems in satellites are very much essential for achieving orbital corrections, altitude control, desaturation of reaction wheels to drag compensation and de-orbiting at the end of life of the spacecraft. Space propulsion can be achieved by chemical or electric methods, each having different performance and adaptability properties. But the efficient and effective method used in state of the art satellite is electric propulsion. Electric propulsion systems make use of electric field to accelerate an ionized gas, to generate the thrust required to give a push for the satellites. Electrostatic propulsion is the most commonly adopted electric propulsion technique and it can be achieved using Hall effect thrusters. Satellites are powered by solar energy and the solar powered batteries can provide a bus voltage which can slightly vary based on angle of incident solar radiation to the solar cell. But each module in these thrusters require different voltage/current inputs. DC-DC converters are used to feed varied voltage values to each of these modules. Aim of this venture is to develop an efficient system to provide power supply for the various important subsystems of hall thruster modules like Anode, Heater, Keeper and Magnet. In the proposed design, the Anode is powered by a phase-shifted full-bridge converter, heater and magnet are powered by buck converter, and the keeper is powered by a boost converter. This work focuses on anode power supply which demands a constant voltage source to power it. Converter topologies were selected as per their ability to provide supply to these modules based on their individual power requirements.

2. EXISTING TECHNOLOGIES

In the electronic systems, there are two mechanisms: analogue and digital. Analogue controllers are used in the system where signals at every point in the system are a continuous function of time. Mainly this controller is consists of resistors, capacitor, transistors, etc. The UC1875 is an example of analogue controller, which is a pulse with modulation controller used in such application. This IC provides control by phase shifting one half bridge with other, by keeping constant frequency PWM. It has 0 to 50% duty cycle. Microcontrollers like Atmega, 8051 series, Aurdino etc., was used earlier where a tradeoff between speed/performance and price can be thought of. For critical applications where speed/performance is of utmost importance, FPGA is used. FPGA is a reconfigurable system that provides a way out to solve complex problems by integrating the speed of hardware with the flexibility of software to enhance system performance.

3. PROPOSED TECHNOLOGY

FPGA represents Field Programmable Gate Array. An FPGA is an IC that can be customized and devised by the embedded systems engineer in the field after it has been fabricated. FPGA is a semiconductor device which is not limited to any pre-characterized equipment work; it is exceptionally habituated in its usefulness and might be organized by the implanted framework engineer as indicated by his structure requirements. FPGAs use pre-constructed logic blocks and programmable channels for implementing custom equipment usefulness depending on how installed framework designers arrange these components. FPGA is field programmable, as FPGAs can be simply reconfigured in the field as specified by new highlights and end client prerequisites. FPGAs are broadly utilized in computerized electronic circuits with implanted frameworks plan acquiring a well characterized place in every developer's tool box [1].

4. DESIGN LAYOUT

4.1 Software

The FPGAs are modified and arranged using hardware description language like Verilog and VHDL which are utilized for an application specific IC (ASIC). In this project, the VHDL program is run using Xilinx software. Here, a pulse width modulation technique is used which generates signals using VHDL according to the varying duty cycle requirements as decided by the closed loop cycle.

The program consists of three sections. The power delivered to the load is controlled using PWM output signal. The PWM output generation has been designed in VHDL [2]. The main parameter which controls the PWM output is the duty D, which is generated after controlling the error through PID controller logic [3]. These signals are then fed to the MOSFET switch of the converter.

The difference between actual output and the obtained output is defined as error. The error based on output from DC-DC converter is fed to the ADC for sampling. Thus error is given by,

Error = Set value – Measured value

The objective of PID controller is to minimize the error overtime by adjusting control variable u(t) such as turning the switch ON and OFF. The PID has the function of minimizing the error at a faster possible rate without having larger overshoots/undershoots in the output along with maintaining stability. The proportional controller improves the stability of the gain, but produces a steady-state error. The integral controller keeps a memory of all the previous errors and it integrates the non-zero value of error and increases the output and thus reduces the steady-state error. The derivative controller increases the damping of the system which results in reducing the peak overshoot thus reduces the rate of change of error [4].

It is necessary to set the error sum to a limit of an integer value to prevent the overflow. The range is assumed from -8000 to 8000. Thus, the modified error is obtained from the PID controller. The proportional, integral and derivative coefficients ($K_p, K_i, \& K_d$) are also assumed.

PID output is the sum of P, I&D generated with the PID logic and that output is stored as DUTY. The DUTY value is already set which varies from 0% to 46%. In VHDL code, values are assigned in the form of hex value, so by converting into hexadecimal it varies from 0 to 2944.

This duty value is fed to the corresponding PWM signal which produces a shift in the width of the PWM output signals. Therefore, the DC-DC converter is designed to operate in a closed control loop in this paper [5].

The program flow chart is shown below,

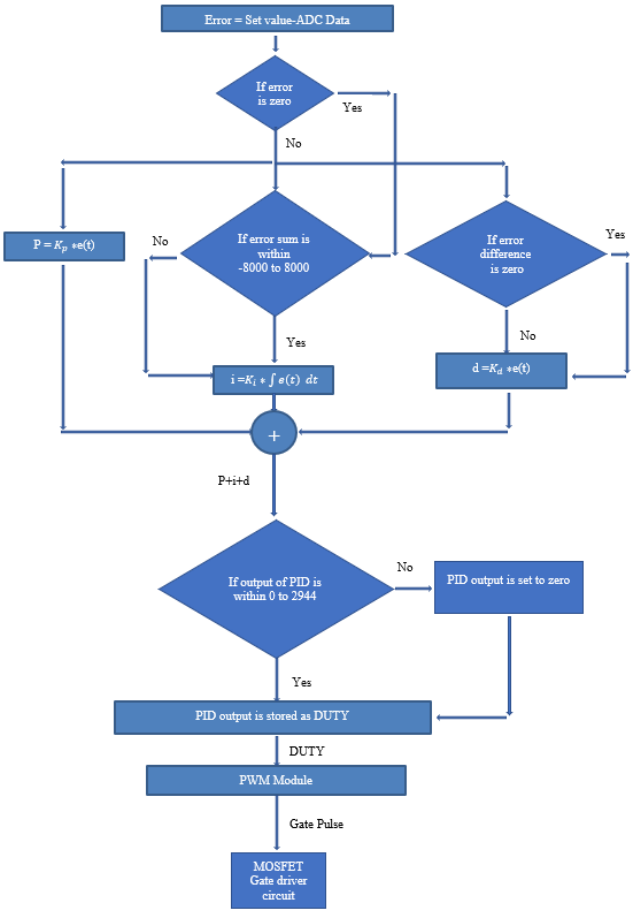

Fig-4.1: Flowchart

4.2 Hardware

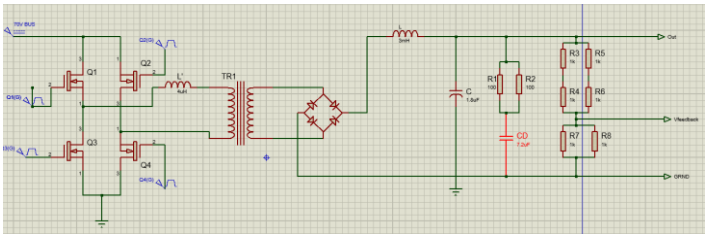

Fig-4.1: Phase Shift Full Bridge converter circuit

Phase-shifted full-bridge converter is designed for the Anode module. The design for the converter is given below:

Anode power supply design

Specifications: V_{out}= 300±5; I_{out}= 1A; 1 Ω at Vin=70V for a switching frequency of 100KHz

TRANSFORMER DESIGN

Core selected- Ferrite core (No: 44416)

For the number of primary turns, N_p

Magnetic flux density, B_m = 0.125T

Core cross section, $A_C = 187mm^2$

$V_{in=} N_p * 4.44 * F_S * B_m * A_C$ Eq (1)

From Eq (1), we get $N_p = 8$ turns

For the number of secondary turns, Ns

Turns ratio, $n= N_s/N_p$ Eq (2)

Duty cycle, D = 90%

$V_{out}= D * V_{in} * n$ Eq (3)

From Eq (3), we get n = 5

Substituting n = 5 in Eq (2), we get $N_S= 40$ turns

INDUCTOR DESIGN

Core selected- Powder core (No: 55351A)

For the Inductance value, L

$I_{out}= 1A$

Duty cycle, D (considering the worst case) = 80%

Time period, $T_s= 10us$

Ripple current, $\Delta I= 20\%$ of $I_{out} = 0.2A$

$L = (V_{out} * (1-D) * T_s) / (\Delta I)$ Eq (4)

From Eq (4), we get L = 3mH

For the number of Inductor turns

Core Inductance per 10 turns, $A_l= 89nH$

$N= [(L * 10^3) / A_l]^{1/2}$ Eq (5)

Substituting L = 3mH in Eq (5), we get N= 190 turns

CAPACITOR DESIGN

Ripple voltage, $\Delta V= 5\%$ of $V_{out}= 2.5V$

Capacitance, $C= \Delta Q/\Delta V$ Eq (6)

Total charge, $\Delta Q= (\Delta I * D * Ts)/16$ Eq (7)

From Eq (7), we get $\Delta Q= 0.1125uC$

Substituting $\Delta Q= 0.1125uC$ in Eq (6), we get

C= 1.8uF

DAMPING FILTER DESIGN

Damping resistance, $R_D= (L * C)^{1/2}= 40.8\ \Omega$ Eq (8)

Damping capacitance, $C_D= 4 * C= 7.2uF$

5. DESIGN ANALYSIS

The result obtained in emulating the code in Xilinx for respective duty cycles is shown in the graphs. The program code is run with duty cycle as input and corresponding pulse width modulated signals are generated.

The graphs for both maximum and minimum duty cycle is shown below,

5.1 At maximum duty 00101110 (46)

When a value less than the reference value is given as input, maximum error is obtained and thus resulting in maximum duty cycle ie., 46.

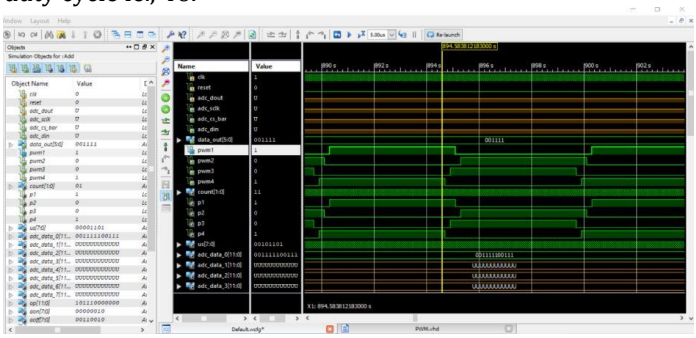

Fig-5.1.1: Simulation waveform at maximum duty

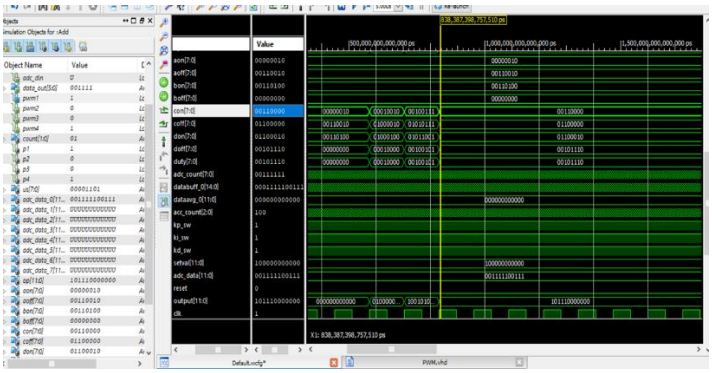

Fig-5.1.2: Simulation waveform at maximum duty

5.2 At minimum duty 00010000 (46)

If a higher value is given as input then the error will be less and results in minimum duty cycle ie., 16.

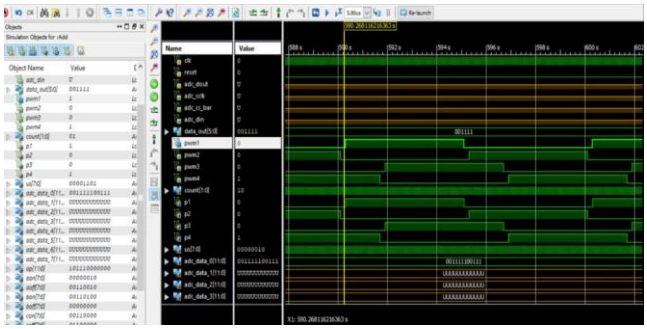

Fig-5.2: Simulation waveform at minimum duty

6. FUTURE SCOPE

Information and resources are provided to assist designers in selecting and evaluating DC-DC Converters for space applications like satellites. An effective design has been included in this paper. The role of FPGA is arising in radar, SIGINT, UAV payloads, military electronics and embedded systems. FPGA plays a central role in High-end military electronics for high performance. In the future, PID tuning can be done effectively by using FPGA, with precise values for PID coefficients, using various tools like MATLAB and so on. Design is done by analyzing the system characteristics.

7. CONCLUSION

All high performance devices require a particular regulated and steady power supply voltage. This can be assured only by a closed loop voltage regulator circuit using control algorithms. This paper presents a digital controller built around an FPGA to control output voltage of DC-DC converters. Here, analog controllers are replaced with a digital controller since those controllers have certain drawbacks such as less flexibility, less tunability and less sensitivity. FPGA is a reprogrammable and compact system in which the controlling is done by pulse width modulation technique. The pulse width is varied using VHDL programming. As user can program according to requirements, possibility of tunability can be imparted to such systems by this approach. These systems have greater scientific scope and can be adapted with respect to developing technologies in near future.

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