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Protection of smart DC Micro Grid using Parameter Estimation Approach

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Abstract - *In a smart DC micro grid, power electronic devices limit the current during fault and therefore, an overcurrent based relaying scheme cannot provide required sensitivity and selectivity for such a system. For a DC micro grid with ring configuration having bidirectional power flow, the protection design is further complicated. The project main objective is to design protection system for the DC micro grid. For reliable supply to customers and to avoid unwanted disconnection of renewable resources, selectivity of a protection scheme is important. Using the direction of fault information of both ends of a line segment in a ring system, internal and external faults are discriminated for network protection. This project proposes the protection model for DC micro grid. Using MATLAB simulations for a ring system, proposed method is tested for various fault situations including high resistance fault, close in fault, signals with noise and considering different modes of distributed generation (DG) operations.*

Key Words: **DC micro grid, transient's analysis, local measurements, fault direction, carrier-aided directional comparison.**

1. INTRODUCTION

Recently significant research and development are being carried out to integrate renewable energy sources(RESs); photovoltaic and wind turbines into existing distribution networks. Growth of energy demand and environmental concern urge for RESs in smart grid initiatives. Today energy policy of many countries envisages increased penetration of RES. Based on the connection of equipment types, networks in the micro grid can be AC, DC or a combination of the two. DC network is more feasible for a demarcated power system, for example, rural power systems, office buildings and ships where the majority of loads are sensitive electronic equipment and electric vehicles. Further advantages with DC micro grid are high efficiency, easy connection of sources to DC bus, negligible transmission loss due to small and localized system, enhanced power transfer capability and interfacing through more efficient power electronic devices.

As there are differences in patterns of voltage and current during fault in DC systems compared to AC, the methods for protecting AC network cannot be copied directly to DC systems. Thus, there is scope of development for improved protection for DC micro grid. Power electronic converters are required to connect both AC and DC sources and loads to a common bus (AC or DC type) in a micro grid system. Moreover, DC network uses less stages of conversion. Internal faults in converter include failure of switches such as insulated-gate bipolar transistor(IGBT).

In a DC network, the common fault is of pole-to-ground type and this is because of physical damage, aging or severe electrical stress in cables. Differential current based protection schemes for cable fault in DC network are proposed in that require reliable communication channel for instantaneous data transfer between protective devices placed at both ends of the cable. Chances of communication failure and loss of data result in performance limitation of differential scheme. The cost of such protection scheme is also a concern in micro grid. unit and non-unit protection schemes are investigated for DC network faults. High rate of rise of fault current and its large steady state value demand for fast operation of DC network protection. The challenge is to avoid damage to the power electronics devices and keep the fault current within interruptible limit, the fault must be cleared in a timely manner. A non-unit protection scheme is proposed for DC network fault detection. The capacitor present in the DC side of the converters supplies current for short duration during a fault in the line. The main drawback of this method is that it shutdowns the system completely for a fault. A fast and selective protection scheme based on direction of current information only for DC network is proposed.

During high resistance fault, flow of current direction may not be indicative of fault direction for a protection system. With increased number of sensors and communication infrastructure, the concept of smart micro grid is being realized for automatic network monitoring and management, increase the usage of intermittent sources and decrease the network congestion. Protection action can be performed utilizing this advanced communication infrastructure of future smart DC micro grid.

In this paper, a protection scheme for smart DC micro grid with ring configuration is proposed. Using local intelligent electronic device (IED), voltage and current data during fault, a LS based technique estimates the inductance of the fault path which is able to discriminate forward and reverse faults with respect to the IED. This fault direction information is communicated to the other end IED of a line

segment. Using the local and other end fault direction information, each IED identifies any internal fault of the line segment correctly. Signals generally being contaminated by noise in a system, as proposed method uses least square filtering, it is able to estimate the seen inductance in IEDs accurately. The method is tested for numerous cases including high resistance and close-in-faults using PSCAD/EMTDC simulation data for a DC micro grid that considers DGs with different modes of operations. The performance of the method is found to be accurate and a comparative assessment shows its strength.

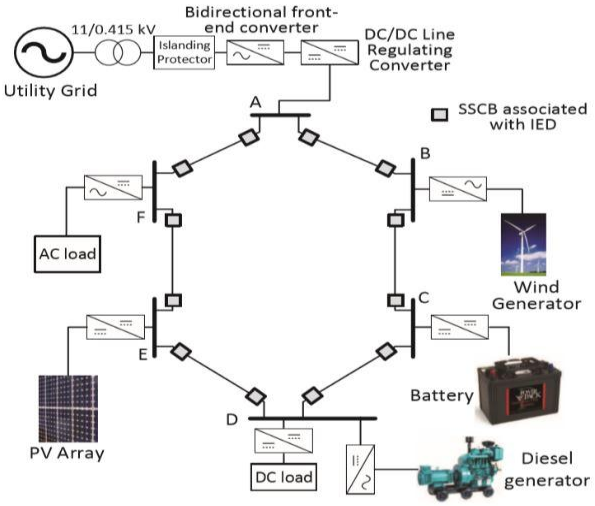


Fig - 1 : DC Micro grid with ring configuration

1.2 FAULT ANALYSIS OF DC MICRO GRID

A smart DC micro grid with ring configuration is considered as shown in Figure. 1. To the micro grid PV array and wind generators are connected which supply power to different DC and AC loads. For efficient and reliable energy management and as a backup, battery is connected to the micro grid. Using bidirectional AC-DC front-end converter and DC-DC converters, integration of sources, loads and storage is done. Grid forming DGs regulate voltage and behave as a slack terminal in the islanded DC micro grid. In this case, diesel generator and battery would act as grid forming sources. PV array and wind turbines operate as grid following sources that injects power under maximum power point tracking (MPPT) mode.

1.1 DC Short-Circuit Fault Analysis

A short circuit fault in DC network is a severe condition for converters and the IGBTs can be blocked for self-protection letting reverse diodes exposed to overcurrent. During fault the network passes through two states. First state is the natural response of the RLC circuit due to discharge of DC link capacitor just after the occurrence of a fault and second state starts when the fault current reaches to peak and capacitor voltage becomes less than the maximum of input voltage, that results the participation from converter interfaces sources and loads to the fault current. Both states are further analyzed below.

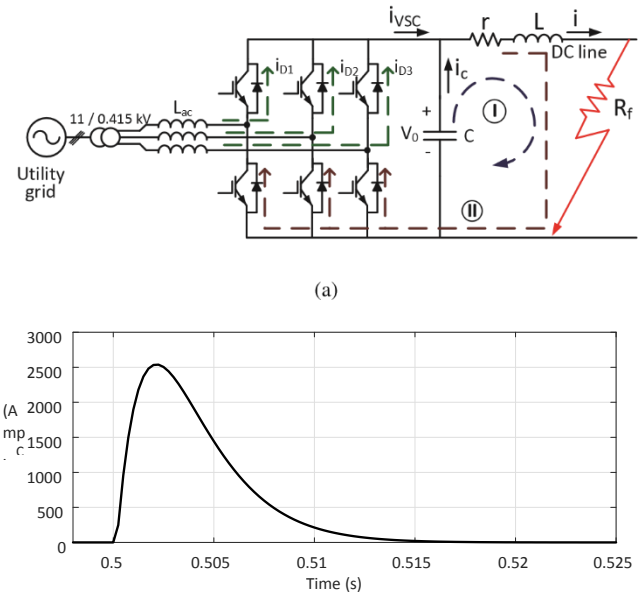


Fig - 2 : (a) Equivalent faulted network of a DC short-circuit fault at VSC terminal (b) Capacitor discharging current during short circuit fault

2.1 Analysis for Capacitor Discharge:

With the onset a fault, the capacitor starts discharging through cable impedance as in the equivalent circuit shown in Fig. 2a. The peak current resulting from the discharging of DC link capacitor discharge is shown in Fig. 2b and the magnitude goes around 10 times of the rated current in a system of 100 kW, 350 V DC, without the operation of any IEDs. Considering the fault inception at time t0, the RLC circuit response in frequency domain can be written as

$$I(S)=\frac{\frac{V_o}{L}+I_o s}{s^2+\frac{R}{L}s+\frac{1}{LC}} \quad (1)$$

where $v_c(t_0) = V_0$, $i(t_0) = I_0$. L and r are the inductance and resistance of the cable from converter terminal to fault point. R is the sum of r and fault resistance. In (1), the contribution of converter current to the fault is not considered due to the slow response of the converter controllers. The voltage across the capacitor and fault current in time domain will be

$$Vc(t)=\frac{V_o w_o}{w} e^{-\alpha t} \sin(wt+\beta) - \frac{I_o}{w_c} e^{-\alpha t} \sin(wt) \quad (2)$$

$$I(t)=C\frac{dV_c}{dt}=\frac{V_o}{wL} e^{-\alpha t} \sin(wt) - \frac{I_o w_o}{w} e^{-\alpha t} \sin(wt-\beta) \quad (3)$$

α = R/2L, $w=\sqrt{\frac{1}{LC}+\left(\frac{R}{2L}\right)^2}$, $w_{0=\sqrt{\alpha^2+w^2}}$ and β = tan−1(ω/α).The form of current response is defined by the relationship between magnitudes of α^2 and ω_0^2. The fault current response will be over, under and critically damped for $\alpha^2 > w_o{}^2$, $\alpha^2 < w_o{}^2$ and $\alpha^2 = w_o{}^2$ respectively. With high DC link capacitance and low inductance of the cable, the predominant part of any underdamped fault current shown in (3) is due to the voltage of initially charged capacitor. Therefore, the expression for fault will now reduce to

$$i(t) \cong \frac{V_o}{wL} e^{-\alpha t} \sin(wt) \quad (4)$$

For highly underdamped response($\alpha^2 << \omega_0^2$ and $\omega \approx \omega_0$), (4) can be further simplified to

$$i(t) \cong \frac{V_o}{Zo} e^{-\alpha t} \sin(w_o t) \quad (5)$$

where Z_0 is the surge impedance of cable up to fault point and is represented as $Z_0 = \sqrt{\frac{L}{C}}$. Time taken by the fault current to reach its peak during underdamped and overdamped cases are as in respectively,

$$t_{pund} = \frac{1}{w_o} \tan^{-1} \frac{w_o}{\alpha} \quad (6)$$

$$t_{povr} = \frac{\ln(n1/n2)}{n1-n2} \quad (7)$$

where $n_1 = -\alpha + \sqrt{\alpha^2 - \omega_0^2}$ and $n_2 = -\alpha - \sqrt{\alpha^2 - \omega_0^2}$.

Using cable parameters and DC link capacitor time to reach peak current during fault is calculated for both extreme cases (solid fault, Rf = 0 Ω and high resistance fault, Rf = 1 Ω) and found that the allowed fault detection time before load voltage collapses in DC system is much lesser compared to AC system.

2.1.1Freewheeling Diode Operation:

The second step of fault current analysis is with the presence of freewheeling diode in parallel with active devices in the converter. This phase starts when the voltage across DC link capacitor drops to zero or becomes negative and it is after tpund or tpovr as defined in (6) and (7). As an effect, the voltage at converter terminal gets reversed and the diode starts conducting as shown in Fig. 3. The diode D represents the equivalent of any conducting leg of converter. The current response changes due to this alternative path irrespective of the IGBT conducting state. Fig. 3c shows the equivalent circuit of faulted network during conducting freewheeling diode. The reverse polarity circulating current can be expressed as

$$i(t) = \frac{V_d}{R_d + r} + A_1 e^{n1t} + A_2 e^{n2t} \quad (8)$$

where A_1, A_2 are the coefficients which depend on initial conditions and n_1, n_2 are the roots as defined in (7), in which the damping factor $\alpha = \frac{r}{2L} + \frac{1}{2R_dC}$ and the resonant frequency $\omega_0 = \frac{1}{\sqrt{LC}} + \frac{r}{\sqrt{R_dLC}}$. The voltage across the parallel branch diode-capacitor will be $v(t) = i(t)r + L\frac{di}{dt}$. Substituting $i(t)$, the voltage can be expressed as

$$v(t) = \frac{V_d}{R_d + r} r + A_1 e^{n1t}(r + n1t) + A_2 e^{n2t}(r + n2t) \quad (9)$$

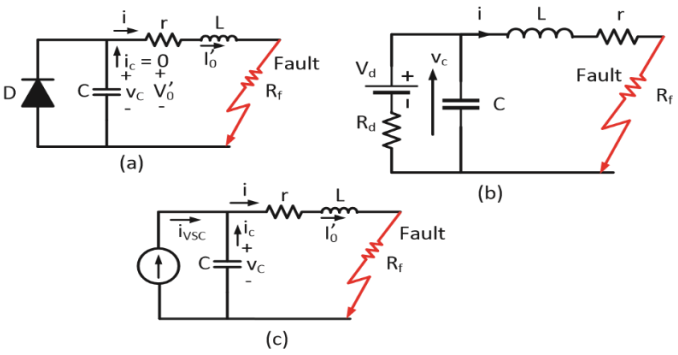


Fig-3: (a) Freewheeling diode operation (b) equivalent circuit of conducting freewheeling diode and (c)current from converter

3. PROPOSED PROTECTION SCHEME

A protection scheme for DC micro grid with ring configuration, as shown in Fig. 1, is presented in this section. The micro grid consists of number of line segments and each segment is having an IED at each end to control the associated solid state circuit breaker (SSCB). The IEDs acquire voltage and current at a sampling rate of 4 kHz. The method estimates the fault path inductance with the onset of a fault which is detected by an index (h). The LS estimation technique provides the seen inductance with negative or positive sign depending on the fault position with respect to the IED; forward or reverse. This information from an IED is communicated to other end IED and vice versa for identifying an internal fault correctly. The proposed protection scheme is for the ring with 6 line segments having 12 associated IEDs. However, number of IEDs can be decided by selectivity, reliability and cost perspectives. Details on the method is provided below.

3.1 Fault Detection:

In a DC system, any disturbance such as fault, load change or a switching phenomenon causes high rate of change of current . To detect such a disturbance and to initiate the main algorithm the change in current information over a period of time is used using local current data. For this, the

disturbance index (h) is calculated from the following relation

$$h = \frac{1}{N\Delta t}\left(\sum_{j=1}^{N}|i_{j+1} - i_j|\right) \quad (10)$$

where ij corresponds to sample value of current and N=5. For 4 kHz sampling, the threshold ξ = 4000 A/s (where Δt is sampling interval and change of current over the period of NΔt is 5 A). When h exceeds ξ, the algorithm triggers the main algorithm where the protection decision is derived. For small disturbance or change in light load where rate of rise of current is slow, the numerator of h is not high enough and h does not exceed ξ. This provides high security in protection decision.

3.2. Protection Arrangement at One End of the Line: Protection arrangement consists of three major parts such as instrument transformers, IED and circuit breaker as shown in Figure 4. In this work, DC bus voltage and line current are sensed using ACPL-C87A and ACPL-C79A respectively. These sensors provide high precision requirements, more transient immunity (15 kV /μ s) and accuracy. IED that receives data from sensors and generate control command for breaker operation is used as relay. For fast operation, SSCB is most suitable for DC networks. Operating time is in the range of 50 μs, which is considered in this work.

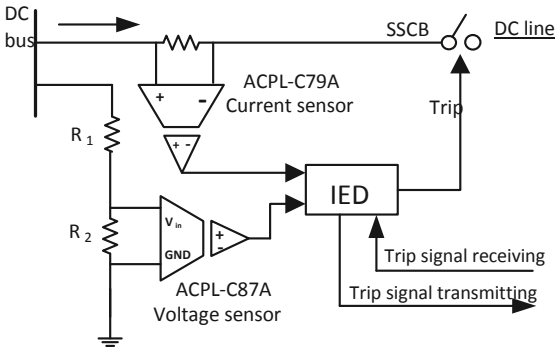


Fig- 4: Protection arrangement at one end of a line in the DC micro grid

3.3 Carrier-aided directional comparison relaying scheme:

Ring type network has gained wide spread acceptance for DC micro grid system as shown in Fig. 1. For such a network, IEDs coordination can be done by using pilot protection scheme. Channel delays on digital microwave are very short, typically 400 to 600 μs, making them suitable for high speed relaying. Using carrier-aided directional comparison scheme, a directional relay can differentiate the internal and external fault.

Transmitting this information to the remote end, both relay can determine whether the fault is in the protected segment or external to it. IED transmits a trip signal (i.e. 1) to the remote end once it sees a fault in forward direction and a block signal (i.e. 0) for reverse fault. A trip is triggered in case IEDs at both ends of the line see forward fault and neither end has received a blocking signal.

The flowchart of the proposed protection scheme is shown in Figure 5. With available measurements, when the disturbance index h exceeds the threshold, estimation of seen inductance at IED is obtained. Finally, trip signal is derived with negative value of inductance on both sides of the line segment.

With desired reliability level of protection system, the investment for protection equipment's must be done. For distribution system operator (DSO) and DG producer, cost of supply interruptions, cost of network losses, outage cost of DGs and power quality penalties are the important considerations. This should be included for economical evaluation of protection system. It is to be noted that, before the final decision concerning the investment a cost benefit study must be conducted.

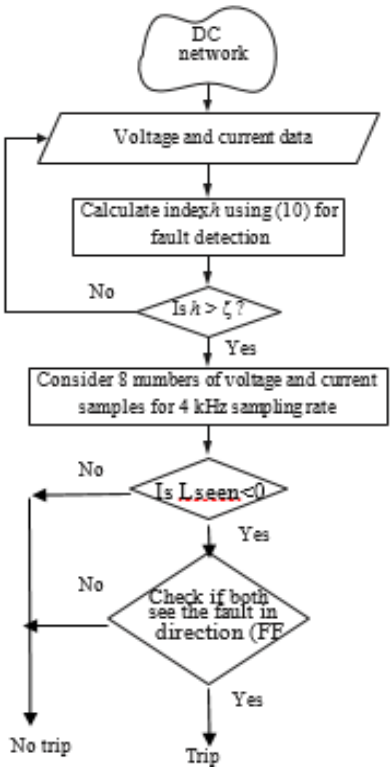


Fig-5: Flowchart for the proposed protection scheme

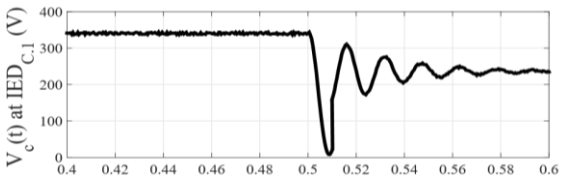
TABLE 1: CIRCUIT BREAKER OPERATION COMMAND BY THE METHOD FOR DIFFERENT FAULTS

Fault in line segment	Estimated direction of fault by IED for different line segments						Decision for SSCB operation in corresponding line segments		
	CD		BC		DE				
	$IED_{C.}1$	$IED_{D.}2$	$IED_{B.}1$	$IED_{C.}2$	$IED_{D.}1$	$IED_{E.}2$	CD	BC	DE
CD	FF	FF	FF	RF	RF	FF	Trip	No trip	No trip
BC	RF	FF	FF	FF	RF	FF	No trip	Trip	No trip
DE	FF	RF	FF	RF	FF	FF	No trip	No trip	Trip

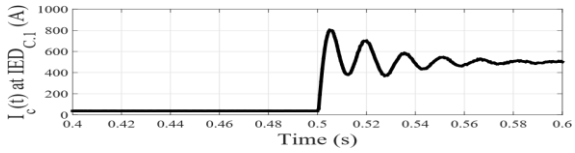
4. RESULT A 350 V monopolar DC microgrid as shown in Fig. 1 is considered for testing the proposed protection scheme. Using PSCAD/EMTDC simulation data are generated for the system by creating faults in different line segments. Voltage and current data are acquired at a sampling rate of 4 kHz for further processing. Proposed method is tested for numerous cases such as forward and reverse faults, close-in-fault, performance under noisy condition.

4.1: Performance of the Method for Faults in Different Line Segments:

A line-to-ground fault with fault resistance 0.1 Ω is created at time t = 0.5 s in the line segment CD (Fig. 1) at 150 m from bus C. Voltage and current through the IEDC.1 are shown in Fig. 6a and Fig. 6b respectively.



(a)



(b)

Fig -6 : For faults in line segment (a): voltage seen by IEDC.1 (b) :current seen by IEDC.1

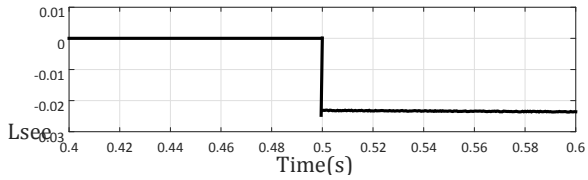
Using carrier-aided directional comparison relaying scheme, if IEDs at both ends of a segment see the fault in their respective forward direction, the fault will be internal, else an external fault. For faults in different line segments the estimated direction of fault by IEDs are provided in Table II. In summary, for the fault in middle of the line segment CD both IEDs (IEDC.1 and IEDD.2) see as forward fault (FF) and thereby a trip decision is derived for associated circuit breaker at the segment.

For this fault, inductance seen by IEDB.1 is -0.023 mH (FF) and that for IEDC.2 is 0.072 mH (RF) and thereby a no trip command is derived for their corresponding circuit breaker operation in the line segment BC. Similar analysis is carried out for fault in line segments BC and DE and, the decision for circuit breaker operation in corresponding line segment is derived.

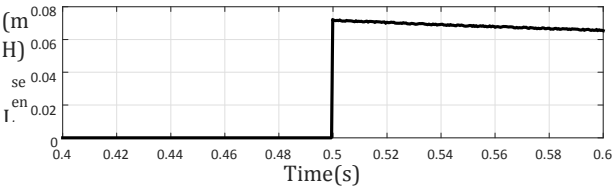
4.2: Close-in-internal fault:

An IED may experience a voltage collapse condition for a fault close to it. The performance of the proposed method is verified for such a case. A line-to-ground fault is simulated in the line segment BC at a distance of 0.2 m from IEDB.1 at 0.5 s and inductance seen by this IED is shown in Fig. 7a. Fault resistance of 1.0 Ω is considered and data acquisition is performed at a rate of 4 kHz.

For a close-in-fault in reverse direction of IEDB.1, the seen inductance is shown in Fig. 7b. Proposed method uses deviation in voltage from pre fault to fault for seen inductance estimation and therefore it is able to identify correctly even for close-in-fault.



(a)

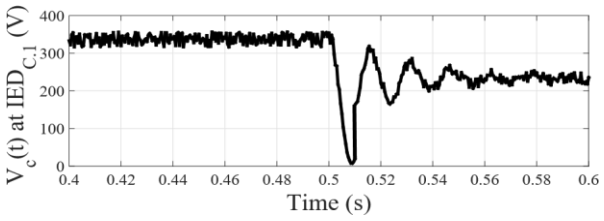


(b)

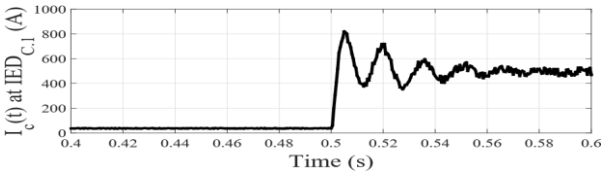
Fig - 7: Inductance seen at IEDB.1 for close-in-fault (a) forward fault (b) reverse fault

4.3 Performance with noisy signals:

The performance of the method is tested for the voltage and current signals contaminated with uniform distribution noise with zero mean and a standard deviation of 2.5%. During such environment, voltage and current through the IEDC.1 for a fault in the line segment CD are shown in Figure 8 With a fault resistance of 0.2 Ω, a line-to-ground fault is created at 0.5 s. From Figure 8, it is clearly observed that method performs well during noisy condition where the inductance value during fault is consistently negative.



(a)



(b)

Fig - 8: Noisy signals seen by IEDC.1 (a) voltage (b) current

5. CONCLUSION

DC micro grid protection with ring configuration is challenging because of current limiting control in converters and bidirectional power flow. In this work, a parameter estimation based protection technique is proposed for smart DC micro grid with ring configuration. The method uses LS technique for estimation of seen inductance at each IED during fault from which forward and reverse faults are discriminated. This fault direction information is communicated to other end IED for identification of internal fault if any in that line segment. The results show the accuracy of proposed method for different fault resistances, close-in-fault and signals contaminated with noise. In a scaled-down laboratory setup, the proposed algorithm is tested and found correct. The performance of the method is found to be better for high resistance fault and for faults during high loading conditions as evident from the comparative assessment.

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