# Multiplexer –Based Design of Adders for Low Power VLSI Applications

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***Abstract* —** In recent trends energy saving circuits have become indispensable in contemporary VLSI design. The prominence in VLSI design has fluctuated from high speed to low power because of the expeditious rise in loads of portable automatic systems. This paper introduces varying techniques for configuring 4-bit Full adder making use of low power 2:1 Multiplexer (MUX). Here a comparative study is made for the operation of 2:1 MUX employing CMOS technology (12T), Pass Transistor Logic (2T) and Transmission Gate Logic (4T). The low power 2:1 Mux is then linked deliberately to get a full adder with sum and carry output. The resulting full adder is then used for implementing 4-bit Full Adder. This paper thus presents, speedy and efficient multiplexer based 4-bit Adder for low power applications like ASIC (Application Specific Integrated Circuits), ALU (Arithmetic Logic Unit). Simulations were performed using Tanner Tool(S-edit, T-spice, and W-edit). The simulation outcomes demonstrate undoubtedly the refinement of the suggested design with reference to reduced power dissipation, less propagation delay, limited occupying area in comparison to other popularly used prevailing adder circuits on the basis of multiplexer**.**

**Keywords—VLSI Design; Multiplexer; low power; high speed: Full Adder; CMOS; 2:1 MUX; Pass Transistor Logic; Transmission Gate Logic ; 250nm Technology Level**

## 1. INTRODUCTION

With the augmentation in laptops, portable distinctive communication systems and the evolvement of shrinking technology, the research endeavour in low-power circuitry has been strengthened and low-power Very Large Scale Integration (VLSI) systems have appeared to be high in demand.

Addition is one of the foundational arithmetic operations and is practiced mostly in several VLSI systems. The main purpose of addition is adding two binary numbers; it is the root of many other functional operations such as subtraction, multiplication, division, and ALU circuits.

Binary Addition can be accomplished utilizing Adders in Logic Circuits. Two types of Adders can be used to conduct the addition namely, Half Adder (HA) and Full Adder (FA). Half Adder can take in two inputs (digits) out of the two Binary numbers under consideration, and generate a Sum and a Carry Out (Cout). But if there is any initial Carry (Cin) from any previous step or previous addition, we need a Full Adder (FA) as it can take 3 inputs and produce the same outputs as the Half Adder (HA).

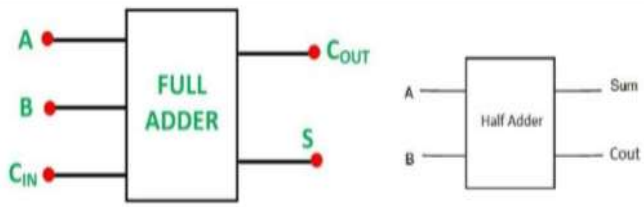



**Figure 1-1** Full Adder and Half Adder (1-Bit)

In order to add two 4-bit Binary digits (variable), we need an arrangement of FOUR interconnected 1bit Adders to execute the summation. The 1st adder can be an FA or a HA depending on the presence of any initial carry (Cin).

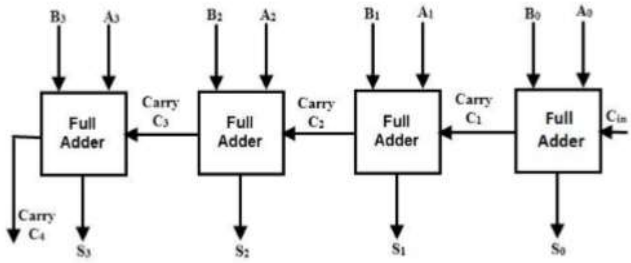



**Figure 1-2** 4-Bit Binary Adder

For our project, we will be using ONLY 2:1 Multiplexers. 2:1 Multiplexers takes two controlled inputs, which are in turn controlled by one selected input. It gives away one output just like every other type of MUX(s).

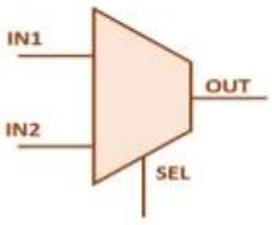
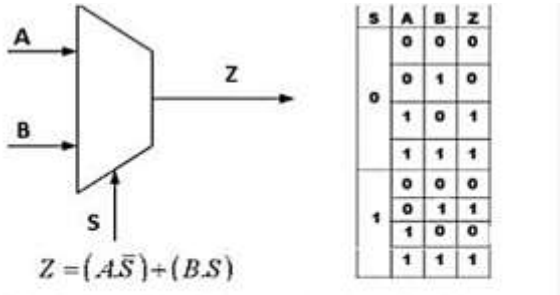



**Figure 1-3** 2:1 Multiplexer

## IL 2:1 MULTIPLEXER

Mux is a data chooser that picks one of the analog or digital input data and redirects the picked data within a single output line. A multiplexer with two data inputs and one control line is referred as 2:1 multiplexer. A multiplexer having $2^n$ inputs has n selected lines and only 1output. Fig 2(a) and (b) respectively show the circuit representation and truth table of a basic 2-to-l multiplexer.




| S | A | B | Z |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| | 0 | 1 | 0 |
| | 1 | 0 | 1 |
| | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| | 0 | 1 | 1 |
| | 1 | 0 | 0 |
| | 1 | 1 | 1 |

Fig.1: The schematic diagram, Boolean equation and the truth table of a 2:1 multiplexer with inputs *A* and *B*, select input *S* and the output *Z*

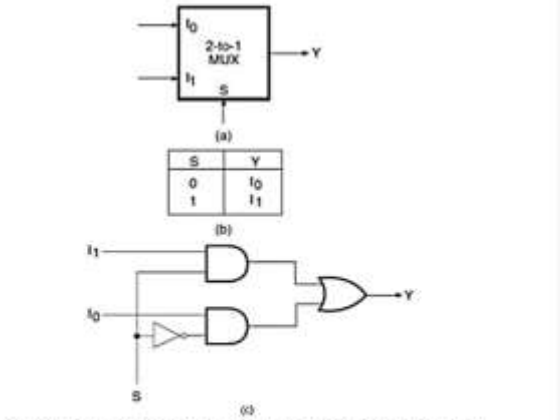
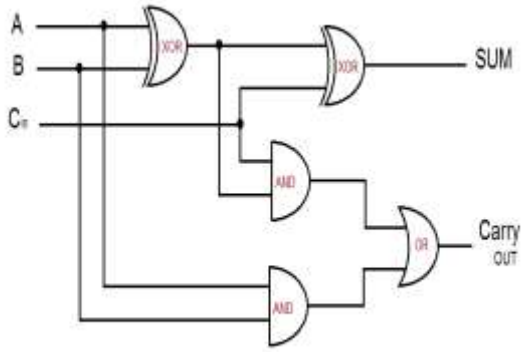



Fig.2:(a) 2-to-1 multiplexer circuit representation, (b) 2-to-1 multiplexer truth table and (c) 2-to-1 multiplexer

Table 2-1 Truth Table (for FA)

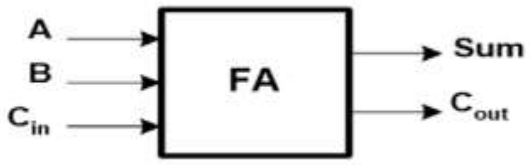
| A | B | $C_{in}$ | Sum | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |




### 111. 1-Bit Full ADDER

The work on this project was initiated by pre-planning, initial drafting and designing the whole circuit before jumping into the implementation and simulation part. It not only made the job simpler, but also paced up the work as we moved through the steps following a pre-set goal.

The very first step of the project was to construct a Truth Table consisting of Two Variable inputs, Carry in (Cin), Sum, and finally a Carry out (Cout). The outputs for the Sum and Cout were derived out from the following Boolean Expressions for the Sum and Cout for an FA as provided by the instructor.




$$Sum = (A \oplus B) \oplus C_{in}$$

$$C_{out} = AB + (A \oplus B)C_{in}$$

**Figure 2-1** Boolean Expression for Sum and $C_{out}$ (for FA)

The Truth Table consists of 5 columns consisting of all the 8 cases of two (variable) inputs namely A and B, Cin, Sum and Cout as follows:

The XOR gate is the elementary unit of full adder circuit. The execution of the full adder can be improved by enhancing the performance of the XOR gate. The main goal of limiting the transistor count is to shrink the dimensions of XOR gate so that massive number of devices can be constructed on a single silicon chip thereby minimizing the area and delay.

### IV. 4-Bit ADDER Using 1-Bit Full Adder

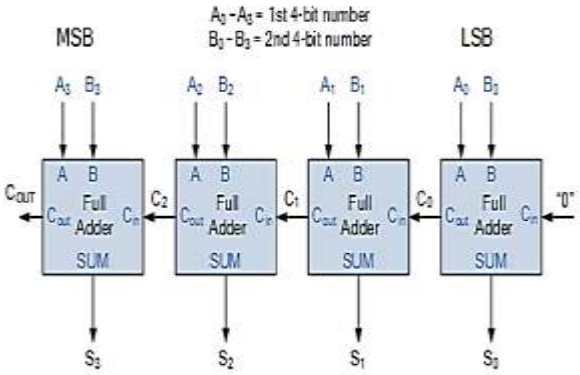
A "ripple carry adder" is commonly "n", 1-bit full adders cascaded in conjunction, with individual full adder portraying a single loaded column in long binary addition. It is exclaimed a ripple carry adder since the carry signals give rise to a "ripple" effect over the binary adder from right to left, (LSB to MSB).

For instance, assume we want to "add" together two 4-bit numbers, the two results of the first full adder will provide the first place digit sum (S) of the addition plus a carry-out bit that functions as the carry-in digit of the next binary adder.

The next binary adder in the series also induces a summated output (the 2nd bit) plus another carry-out bit and we can continue adding more full adders to the amalgamation to add larger numbers, associating the carry bit output from the first full binary adder to the next full adder, and so forth.

The structure of a ripple carry adder is easy and direct; which permits brisk design time; however, the ripple carry adder is proportionately slow, since each full adder must

halt for the carry bit to be calculated from the preceding full adder.




The ripple carry is probably the simplest architecture for an adder. In this architecture the delay simply propagates from one Full-adder to the next one, therefore the employment of the full adder is all that matters in its design.

**V. Design and simulation results of 2:1 Mux adopting various Methodologies**

A logic style is the strategy how a logic function is build using transistors. It dominates the speed, area occupied, power dissipation and wiring complexity of a circuit. All these attributes may differ substantially from one logic style to another style and accordingly make the proper choice of logic style vital for circuit performance.

**A. Complementary CMOS Logic style:** Any task in complementary CMOS is obtained by NMOS pull-down and PMOS pull-up networks bridged between gate, output and power cables.

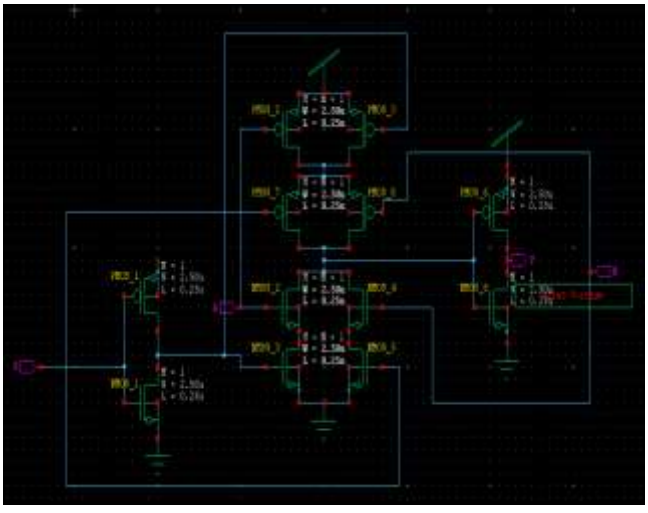


**Figure-** Schematic of 2:1 Mux employing CMOS Technology

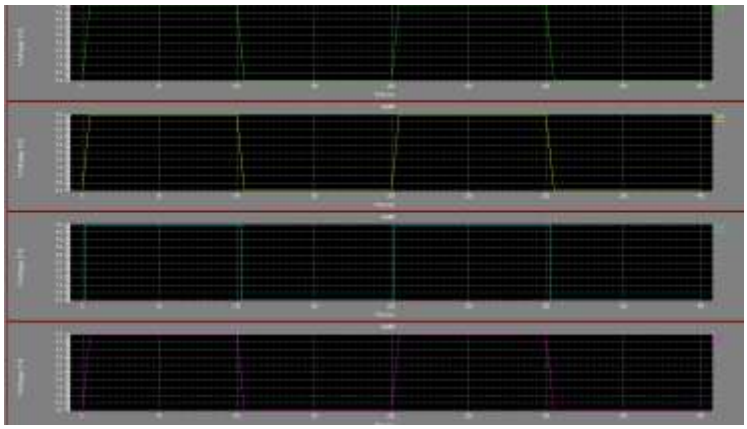


**Figure**-Simulation of 2:1 Mux employing CMOS Technology

**B. Pass Transistor Logic:** The pass-transistor logic minimizes the number of transistors needed, by granting the primary inputs to steer gate terminals in conjunction with source-drain terminals. The superiority is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation. Mostly we are selecting NMOS transistor for establishment.

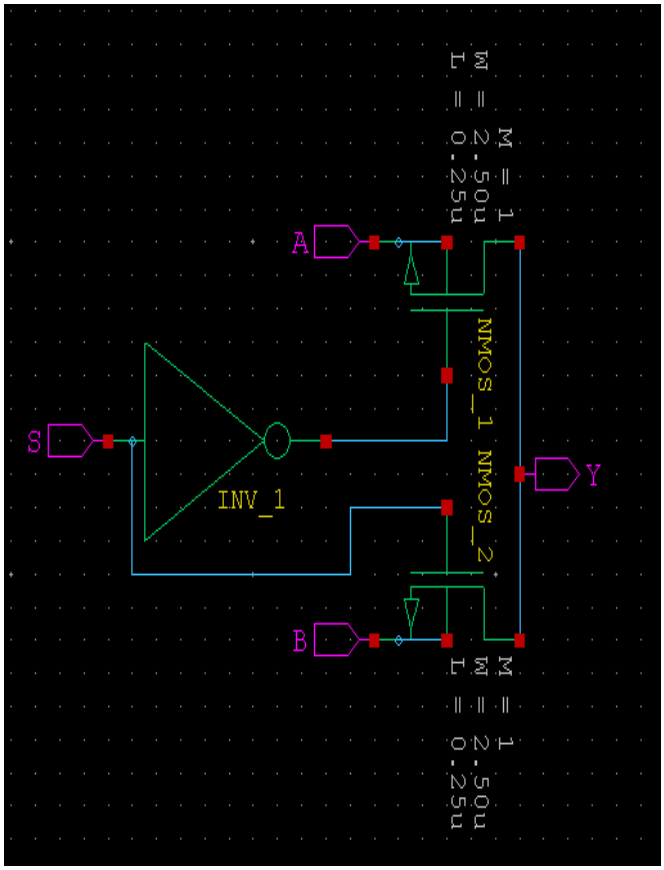



**Figure:** Schematic of 2:1 Mux employing Pass Transistor Logic

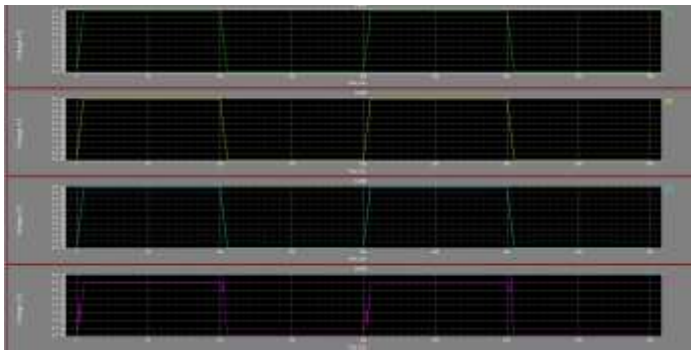
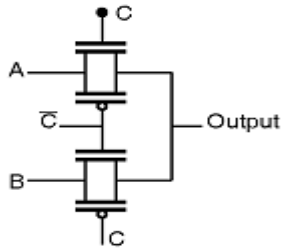


**Figure**-Simulation of 2:1 Mux employing Pass Transistor Logic

**C. Transmission Gate:** When the control signal C is high i.e. at "logic 1" then the uppermost transmission gate operates and it sweeps A over it so that output is A. When the control signal C is low i.e. at "logic 0" then the uppermost transmission gate shuts OFF and it will not let A to sweep over it, simultaneously the lower transmission gate operates and it allows B to sweep over it so the output is B.




**2 : 1 MUX using transmission gate**

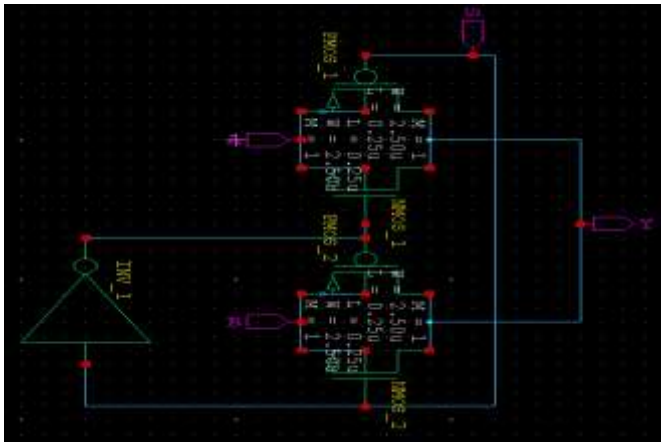


**Figure:** Schematic of 2:1 Mux employing Transmission Gate

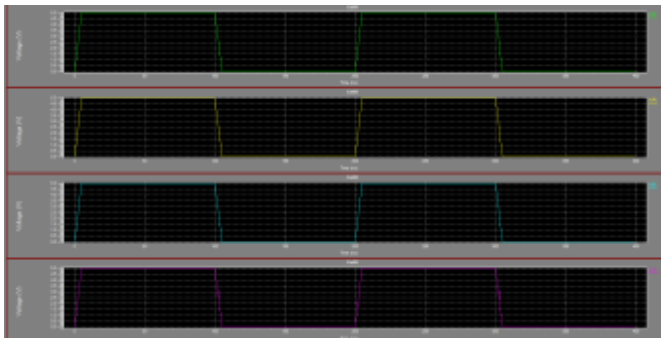


**Figure**-Simulation of 2:1 Mux employing Transmission Gate

On account of power and delay, analysis is done on 250nm technology and for supply voltage 5V

| Logic Type | Power | Delay | Transistor Count |
|---|---|---|---|
| **CMOS** | 2.8358e-004 | -6.2412e-010 | 12 |
| **Pass Transistor** | 3.4412e-005 | 1.5364e-009 | 2 |
| **Transmission Gate** | 3.3751e-005 | 3.1226e-012 | 4 |

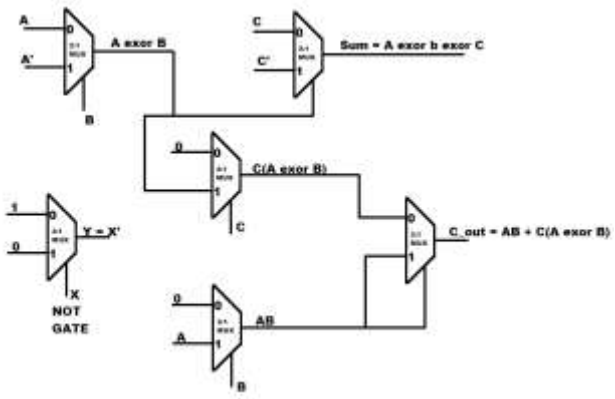
**Table**- Comparison between various methodologies for the enactment of 2:1 MUX

From the simulation outcomes it is discovered that 2:1 MUX using Transmission gate is the most adequate since it has the minimum power wastage and delay.

Therefore, implementation of Full adder is most suitable by Transmission Gate 2:1 MUX.

### VI. Proposed Design for 1-bit Full Adder and 4-bit Full Adder using 2:1 MUX

To implement 1-bit Full adder; first of all 2:1 Mux practicing transmission gate is designed. Then we generate symbol for this 2:1 Mux and use this representation for the further implementation. The implementation is done in the following manner:



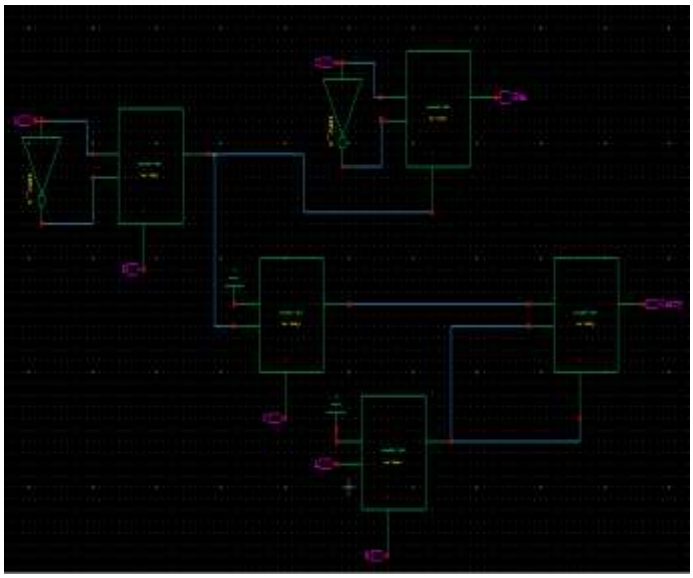


**Figure:** Design of Full Adder using 2:1 Mux

To implement 4-bit Full adder utilizing the above full adder we generate symbol for full adder and use this symbol in a new cell for designing 4-bit full adder.

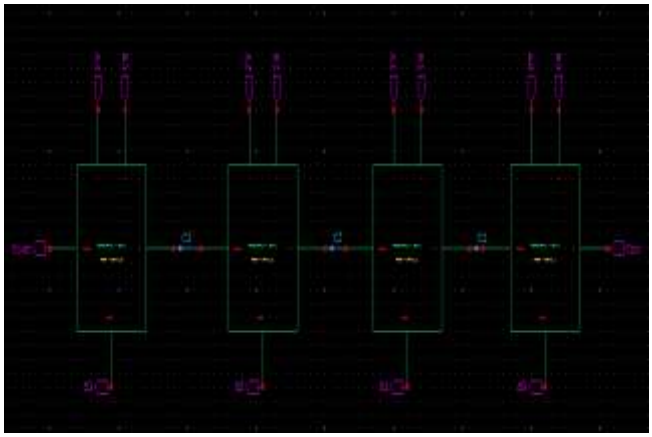


**Figure**-Design of 4-bit Full adder

Thus, these designs of 1bit and 4bit adders are then used for simulations and comparisons between adders of CMOS, Pass transistor and Transmission Gate logic.

### VII. Simulation Results for 1bit and 4bit Full Adders using 2:1 Mux designed with different approaches

Simulations in this project are done using Tanner Tool. The schematic is prepared with S-Edit, the waveform is seen using W-Edit whereas the power and delay is seen with T-spice.

To check the waveforms first of all we have to go on setup simulation and change the settings and then go to run option.

Based on power and delay, analysis is done on 250nm technology and for supply voltage 5V

The simulation Outcomes are as follows:

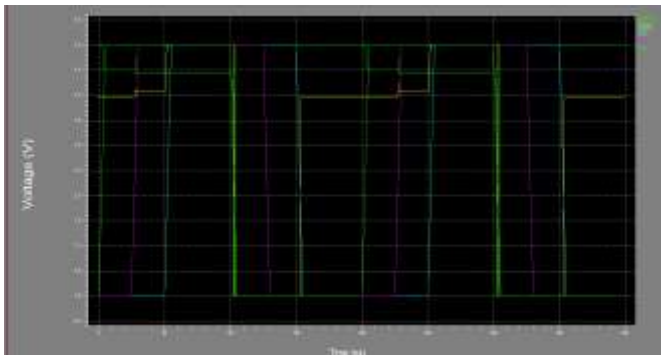


**Figure (a) – Simulation of adder using CMOS**

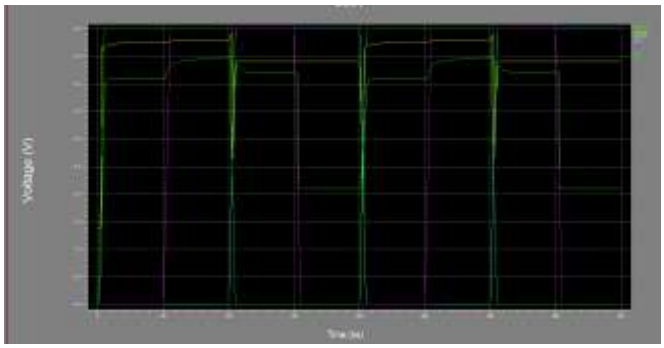


**Figure (b) – Simulation of adder using PASS TRANSISTOR**

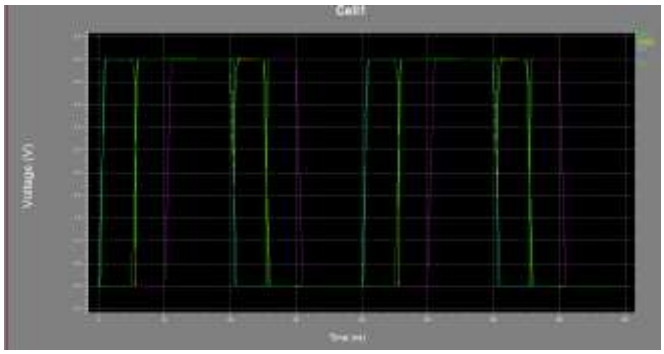


**Figure (c) – Simulation of adder using TRANSMISSION GATE**

Figure (a, b, c) above represents waveforms of 1-bit Full Adder using various Methodologies.

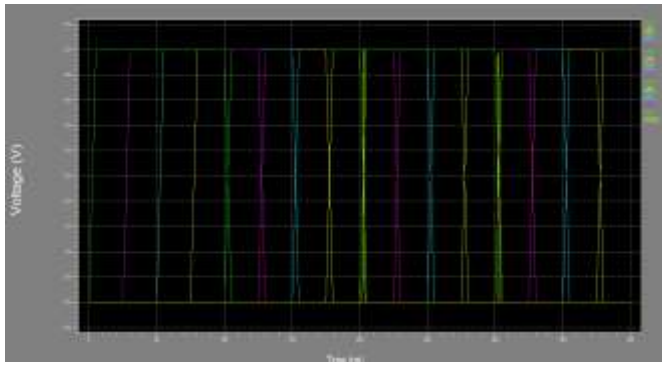


**Figure (a) – Simulation of 4-bit adder using CMOS**

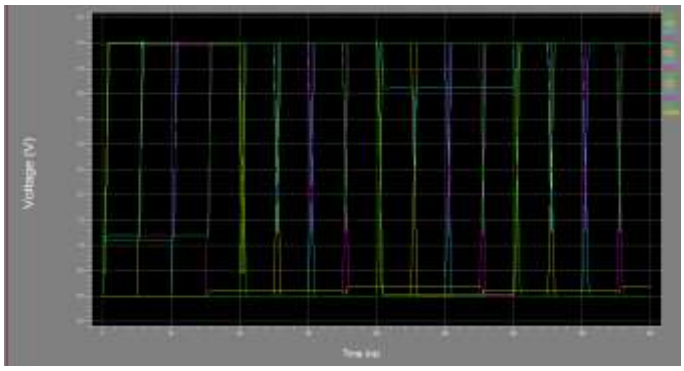


**Figure (b) – Simulation of 4-bit adder using PASS TRANSISTOR**

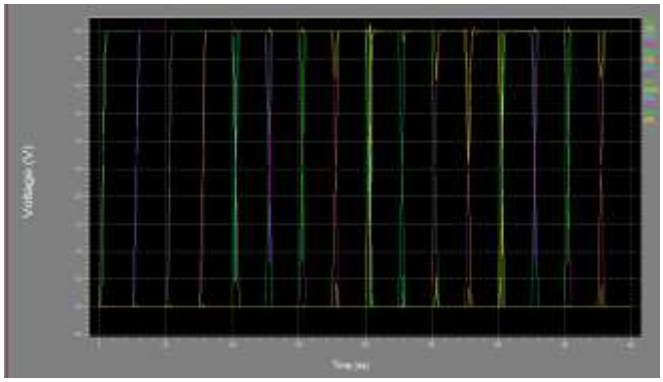


**Figure (c) – Simulation of 4-bit adder using TRANSMISSION GATE**

Figure (a, b, c) above represents waveforms of 4- bit Full Adder using various Methodologies.

| Logic Type | Power | Delay | Transistor Count |
|---|---|---|---|
| **CMOS** | 1.8867e-002 | 1.5053e-007 | 12 |
| **Pass Transistor** | 4.6192e-003 | 2.0691e-010 | 2 |
| **Transmission Gate** | 1.1225e-003 | 2.6337e-010 | 4 |

**Table**- Comparison between varying methodologies for the designing 1-bit Full Adder

| Logic Type | Power | Delay | Transistor Count |
|---|---|---|---|
| **CMOS** | 1.9817e-003 | 1.9988e-007 | 12 |
| **Pass Transistor** | 2.4792e-002 | 4.6391e-010 | 2 |
| **Transmission Gate** | 2.9646e-003 | 2.7506e-010 | 4 |

**Table**- Comparison between varying methodologies for the designing 4-bit Full Adder

## VIII. CONCLUSIONS

From the simulation outcomes it is examined that 4-bit Full Adder using Transmission gate 2:1 MUX is the most coherent adder as it has the most optimized power dissipation and delay. Therefore, it is the fastest adder among 2:1 multiplexers of CMOS, Transmission Gate and Pass Transistor Logic.

Reduction in power consumption delivers several benefits like minimal heat is generated, which minimizes the complications related with high temperature, as this required demand for the heat sinks. This delivers the user with a product that charges less. An additional benefit of the reduced power consumption is the enlarged life of the battery in battery-powered systems.

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