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7- LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

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Abstract - .In this paper a "7 level Cascaded H bridge Multilevel Inverter" is proposed. Since Conventional multilevel inverters (MLI) required big wide variety of capacitors, diodes, electricity switches and input sources. So as to overcome this drawback, proposed single phase MLI can be employed. Proposed MLI includes single source, less range of switches, diodes and capacitors, total harmonic distortion, and harmonic spectrum. For this reason proposed Cascaded Multilevel Inverter reduces the complexity of circuit layout. As such per simulation result as we increase the voltage level of inverter, the harmonics will reduced. On this paper 7-level MLI is proposed for photovoltaic based high power applications also suited for electrical drives and renewable energy applications with stage moving SPWM (sinusoidal pulse width modulation) technique with the help of simulation by using MATLAB/SIMULINK and implementation of Seven level cascaded H-bridge multilevel inverter.

Key Words: MLI Simulation, SPWM method, THD, Comparison between 3-level, 5-level and 7-level.

1. INTRODUCTION

A multilevel inverter is power electronics device this is used for high-power high-voltage utilization consisting of Uninterruptible power supplies, Flexible AC transmission systems (FACTS). Whereas traditional two stage inverter have some boundaries in high-strength high-voltage applications and also involves high switching losses. Multi-level energy conversion is permitted for greater than two voltage tiers to acquire smoothen and minimize distorted dc to ac power conversion and it has got the capability to generate multilevel voltage waveform with much less distortion, less switching frequency and better performance. The stepped waveform is synthesized by way of more than two voltage degrees produced via connection of proper loading. This connection is accomplished with the aid of the precise switching within the power semiconductors. To acquire a quality output voltage waveform they require excessive high switching frequency involving various kind of pulse-width modulation techniques. Multi-stage inverter offers several advantages over two-stage inverter in order to improve the output voltage waveform, minimized (dv/dt) voltage strain on the load and also reduces electromagnetic interference issues, but it has a few demerits. One of the maximum apparent disadvantages is the requirement of higher number of electricity semiconductor switches. Each switch requires a gate driving circuit, consequently maximize the complexity and size of the complete circuit.

The multilevel cascaded H-bridge (CHB) inverter shown in figure is one of the famous inverter topologies as it can operate on high voltage and has low dv/dt with reduce general harmonic distortion (THD) and modular structure for reduced production cost. The traditional modulation schemes for the CHB inverter involves multilevel carrier primarily based sinusoidal modulations with phase opposition disposition techniques. The level-shifted modulation schemes have a very good THD profile, but suffer from unbalanced energy distribution, while the phase shifted schemes are less difficult or we can say simpler but produce high overall harmonic distortion (THD).

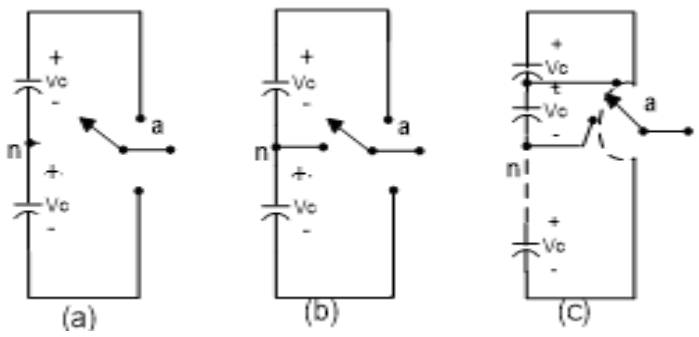


Figure 1: one phase leg of inverter (a) two level (b) three level (c) n-levels

2. MODULATION TECHNIQUE

There are numerous modulation techniques for multi-stage inverters. Multilevel inverter has to synthesize a sinusoidal waveform by using the modulation technique to get the controlled output voltage.

[A]. Sinusoidal pulse width modulation (SPWM) method is easy and efficient. The excessive wide variety of switches composing a multilevel converter may also lead to the belief that complex algorithms are vital. The modulation algorithm used to force the multilevel converter has to be aimed to present the voltage level required for every leg; the interpretation within the right transfer configuration is done via other algorithms which may be hardware or software implemented. The modulation strategy used right here is the multicarrier service overlapping pulse width modulation

[B]. In the scheme Phase opposition disposition modulation all the carrier waves which are above the 0 reference are in phase and is one hundred eighty (180) degree out of phase with the ones below zero (0) reference. The law or convention for the phase opposition disposition technique, that the range of level N = five. The N–1 = 4 carrier wave shapes are controlled such that which are above reference zero are in phase and are 180 out phase with the ones underneath zero.

1. The converter switches to +Vdc/2 if the reference is grater or higher than all carrier wave forms.

2. The converter switches to Vdc/four if the reference is less than the top upper carrier waveform and higher than rest of all other waveforms.

3 The converter switches to 0. If the reference is less than the two upper top carrier waves and higher than two lowest carrier ones.

4. The converter switches to -Vdc/four if the reference is greater than the two lowest carrier wave shapes and lesser than all other carrier waveforms.

5. The converter switches to -Vdc/2 if the reference is lower than all the carrier waveforms.

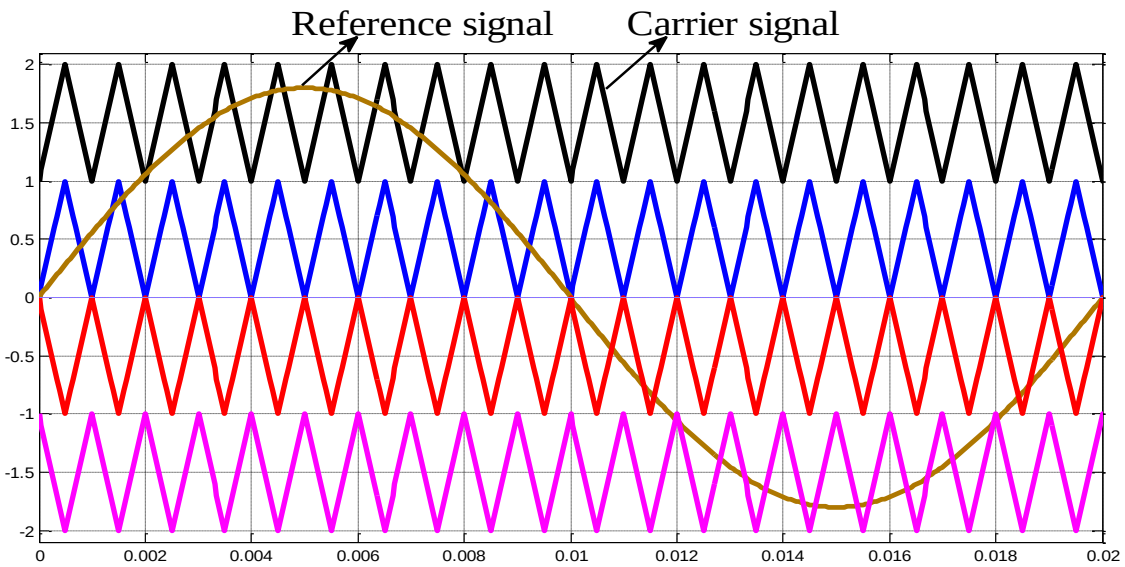


Fig. 2: Carriers and modulating signals at mf = 20, ma = 0.9

3. PROPOSED METHODOLOGY

In this proposed system we have series connected seven-level CHB to lessen or reduce the switch count and minimize THD. The main of the proposed device is inverter presents higher quality output with reduced strength loss as compared to the other conventional inverters when compared with same output quality. The overall block diagram for the proposed inverter is shown in fig.3 and the waveform of the proposed method is also shown.

Inverter topology is as shown in fig.4. When comparing with the existing multi stage inverters, the new MLI inverters can successfully reduce the switch count and also the number of gate drivers as the no. Of voltage degrees or levels increases. For a given no. Of voltage Degrees (level) m, the new inverter requires m+3 active switches. More or less half of the no. Of switches, clamping diodes, and Voltage-splitting capacitors inside the diode clamped Configuration or clamping capacitors within the flying capacitor Configuration. The comparison of the proposed MLDCL Inverter and cascaded inverters based totally on requirements of number switches and number of levels. From this evaluation it's far clear that because the level of voltage stages, m, grows, the count of switches will increase in line with m+3 for the Inverter, compared to two (m-1) for the cascaded H-bridge Multilevel inverters.

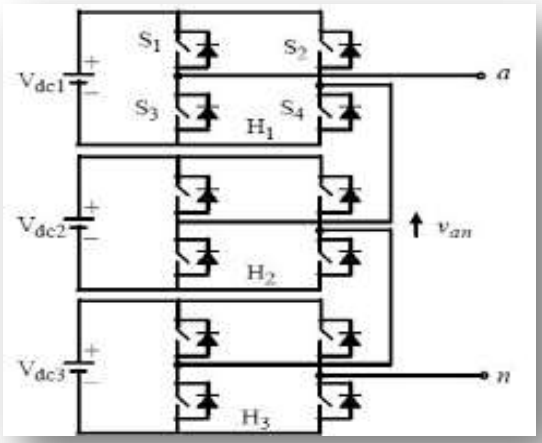


Fig. 3. Cascaded H-bridge 7-level Inverter

Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
0Vdc	1	0	1	0	1	0	1	0	1	0	1	0
Vdc	1	0	0	1	0	0	1	1	0	0	1	1
2Vdc	1	0	0	1	0	0	1	1	1	0	0	1
3Vdc	1	0	0	1	1	0	0	1	1	0	0	1
-Vdc	0	1	1	0	1	1	0	0	1	1	0	0
-2Vdc	0	1	1	0	0	1	1	0	1	1	0	0
-3Vdc	0	1	1	0	0	1	1	0	0	1	1	0

Fig. 4. Switching Sequence of Cascaded H-bridge 7-level Inverter

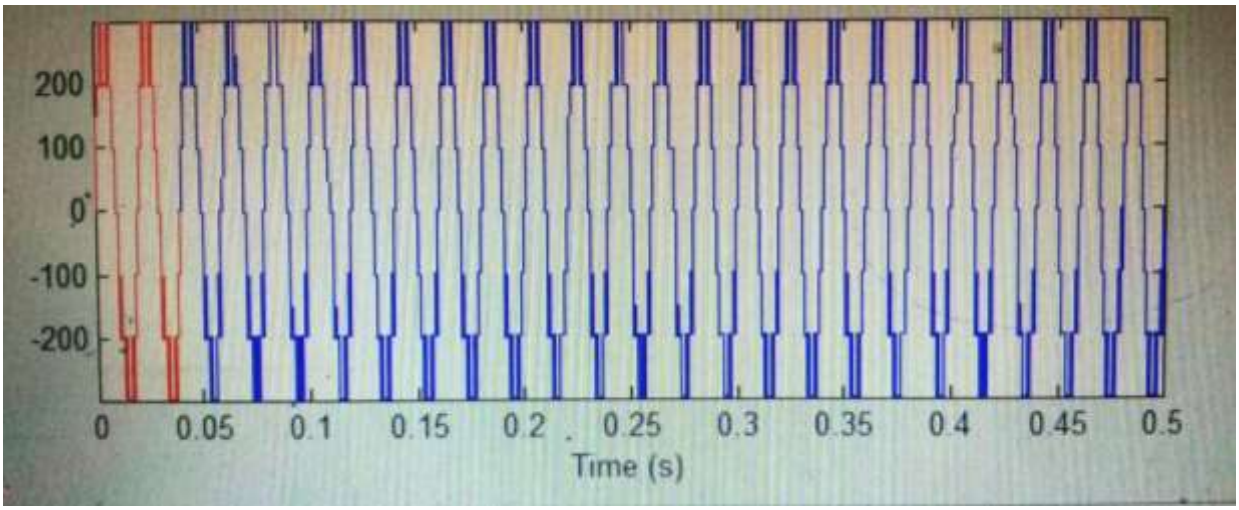


Fig. 5. Waveform of Cascaded H-bridge 7-level Inverter

4. COMPARISON BETWEEN 3-LEVEL, 5-LEVEL AND 7-LEVEL BASED ON TOTAL HARMONIC DISTORTION (THD)

In cascaded H-Bridge multilevel inverter, if number of levels increases then the harmonic distortion is decreases. The THD in 5-Level inverter is less as compared to 3- Level inverter also the THD in 7-level is less as compared to 3- level & 5-level inverter. As the number of voltage levels increases then the output voltage waveform will obtain as like a sinusoidal including number of staircase waveform.

Fig. 6. THD of 3-Level R-Load

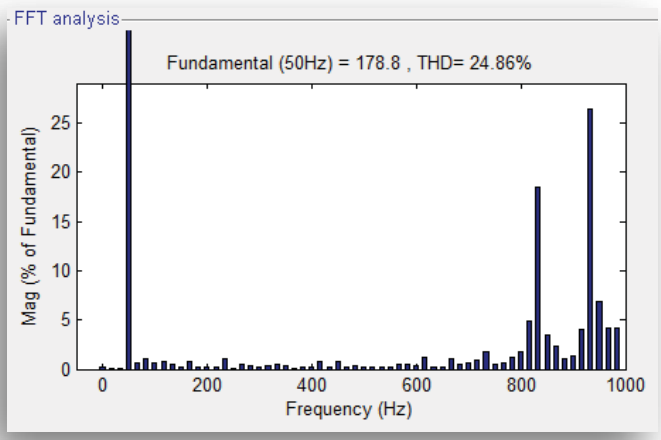


Fig. 7. THD of 5-Level R-Load

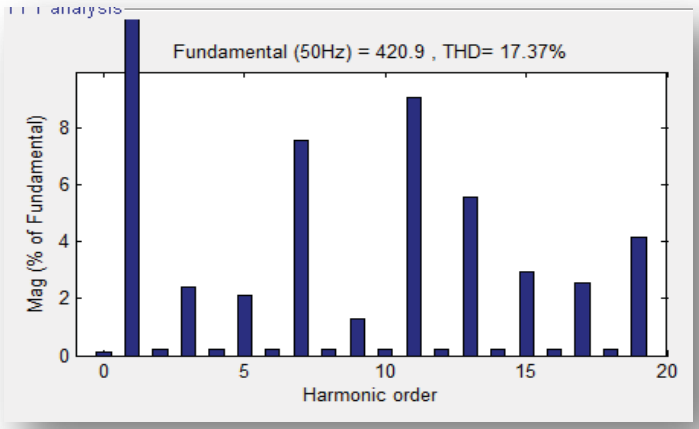
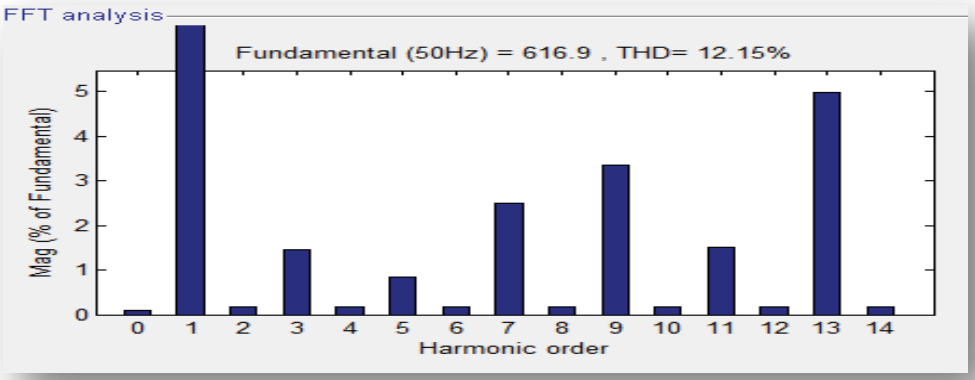


Fig. 8. THD of 7-Level R-Load



5. CONCLUSION

Multi-level cascaded H bridge inverters 7- level has been simulated using MATLAB/Simulink. The following conclusions can be made from the analysis-

As we increase the level of CMLI, the Total Harmonic Distortion content gets decrease as expected. Thus it eliminates the need for filter. Though, THD decreases with increase in number of levels, some lower or higher harmonic contents remain dominant in each level. These will be more dangerous in induction drives. Hence the future work may be focused on implementing closed loop control with suitable harmonic elimination.

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