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Comparison of Symmetric and Asymmetric Cascaded H-Bridge Multilevel Inverters using Multicarrier PWM technique

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Abstract - *Multilevel inverters have become a promising power conversion technology for number of applications in renewable energy systems, flexible ac transmission systems and high voltage direct current systems. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly as voltage stress on the switch increases its lifespan gets decreased. As a result, a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations. The three main topologies in Multilevel inverters are Diode clamped(Neutral clamped), Flying capacitor(capacitor clamped) and cascaded H-Bridge type. Of the above mentioned three the cascaded H-bridge has become popular due to its simpler design and modular property. Further the cascaded H-bridge type can be classified into two types on the basis of equality of input DC sources into Symmetric and Asymmetric cascaded inverters. This paper presents the comparison of symmetric five level inverter and Asymmetric seven level inverter. The symmetric topology consists of two equal DC sources and the Asymmetric topology consists of two DC sources which are in the ratio of 1:2. The two topologies are simulated in MATLAB/Simulink and the results are obtained by connecting these topologies to asynchronous induction motor.*

Key Words: Multilevel inverters, Symmetrical, Asymmetrical cascaded H-bridge multilevel inverters, Total Harmonic Distortion(THD), Carrier based Level shifted Pulse width modulation(PWM).

1. INTRODUCTION

Multilevel inverters include an array of power semiconductors and DC voltage sources, the output of which generate voltages with stepped wave forms. The commutation of the switches permits the addition of the DC voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

Multilevel inverters are more advantageous than two level inverter owing to their,

- Quality power output with reduced Harmonic content
- High voltage handling capability
- Low Electromagnetic Interference(EMI)
- Low switching losses and Higher efficiency

The diode clamped multilevel inverter topology uses diodes to clamp the DC bus voltage to achieve steps in the output voltage. But diode clamped topology has the disadvantage of the capacitor imbalanace where each capacitor is required maintain the voltage which demands a control circuit to ensure this. Also their is a quadratic relation between the number of diodes and output levels to be produced, which for higher levels make the circuit cumbersome.

The flying capacitor topology uses capacitors to clamp the DC source voltage to produce the stepped output voltage. This topology require a large number of storage capacitors and also require a separate circuit to track the voltage across the capacitors and the requirement of more number of capacitors make the circuit bulky and costly.

The third type cascaded H-bridge is formed by the series connection of single phase inverters or H-bridges(see Fig 1.0). These are also referred as 'multicells'. Each multicell is capable of producing three output voltage levels. If 'V_{dc}' is the input DC source then the possible output voltage levels are '$+V_{dc}$', 0 and '$-V_{dc}$' , and cascading of such cells with the employment of suitable control mechanism (multicarrier PWM, Space vector modulation, Selective harmonic Elimination) can produce varied output levels with reduced harmonic content.

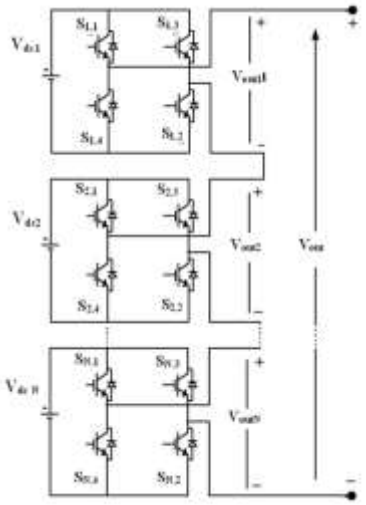

Fig 1.0 Cascaded H-bridge Multilevel inverter with 'N' multicells.

The cascaded multilevel inverter shown in the fig 1.0 has 'N' multicells each with Separate DC source (SDCS). This can be further classified into Symmetric and Asymmetric type.If the DC sources shown in the Fig 1.0 are equal then it is called as Symmetric type, i.e.each cell has same magnitude of DC source connected across its input terminals and is similar to the adjacent cell,whereas in asymmetric type the DC sources shown in the Fig 1.0 are unequal rather they are in the ratio 1:2 (or) 1:3.If the ratio is 1:2 then it is called as binary Asymmetric and if the ratio is 1:3 then it is called as trinary/ternary Asymmetric.

2. SYMMETRIC CASCADED H-BRIDGE MULTILEVEL INVERTER

From fig 1.0 it can be deduced that for symmetric cascaded inverter since all the sources are equal Vdc1=Vdc2=Vdci=VdcN; where i=1,2...N, where 'N' is the total number of H-bridges. Since each cell is capable of producing three output voltage levels, the addition of another identical cell adds extra two levels to the whole inverter output. Therefore number of bridges/cells in a symmetric cascaded inverter gives the number of levels that can be produced from the circuit setup and the relation is as follows, if 'N' be the number of multicells then the number of output levels 'm' that could be produced is m=2N+1,

And the number of switches required is 4*N and the maximum output voltage is Vmax= N*Vdc .

From the above synopsis it can be calculated that for a Five level output, the number of multicells required are 2 with equal DC sources.

Hence two H-bridges are required to generate 5 level output as shown in Fig 2.0

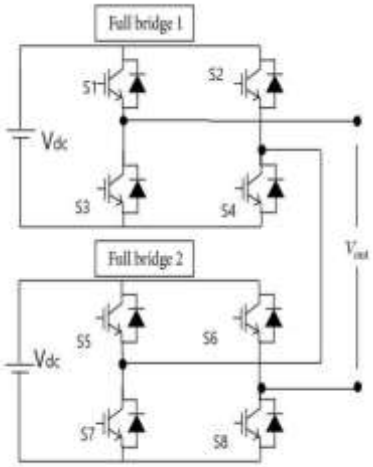

Fig 2.0 Symmetric cascaded five level inverter

The five level output is generated by the optimum control of the outputs of the individual multi-cells, which involves swictching ON and OFF the respective switches such that the corresponding cell responds to a change as required in the output stepped waveform. Likewise the switching states for the power switches in a five level inverter are as shown in Table 1.0

Table 1.0

voltage level(V_{out})	S1	S2	S3	S4	S5	S6	S7	S8
+2Vdc	1	0	0	1	1	0	0	1
+Vdc	0	0	1	1	1	0	0	1
0	1	1	0	0	0	0	1	1
-Vdc	0	0	1	1	0	1	1	0
-2Vdc	0	1	1	0	0	1	1	0

Consider the Full bridge 1 from Fig 2.0, for the bridge output to be zero, the either the switches (S1S2) or (S3,S4) are turned. Hence there are two possible output combinations for zero output level and only one combination is selected on the basis of ease of design of control strategy.

3. ASYMMETRIC CASCADED H-BRIDGE MULTILEVEL INVERTER

In an asymmetric cascaded multilevel inverter the input DC sources are unequal rather they are in ratio (e.g. 1:2 or 1:3) . Asymmetric cascaded type generates more levels at

the output fewer number of switches compared to symmetric cascaded type.From fig 1.0 if the topology assumed is asymmetric i.e. sources are in a ratio of 1:2, then the Dc sources are Vdc, 2Vdc, 4Vdc, 8Vdc,..2^{N-1}Vdc., where 'N' is the total number of H-bridges. Unlike symmetric type,the power semiconductor switches in asymmetric cascaded type are subjected unequal off state voltages. If 'N' be the number of cells in a asymmetric cascaded multilevel inverter,then the number of output voltage levels 'm' that could be generated is m=2^{N+1}-1 the number of switches required is 4*N the maximum output voltage obtained across the terminals is Vmax=(2^N-1)Vdc.

From the above synopsis it can be calculated that for a seven level output, the number of multicells required are 2 with DC sources in the ratio 1:2.

Hence two H-bridges are required to generate 7 level output as shown in Fig 3.0

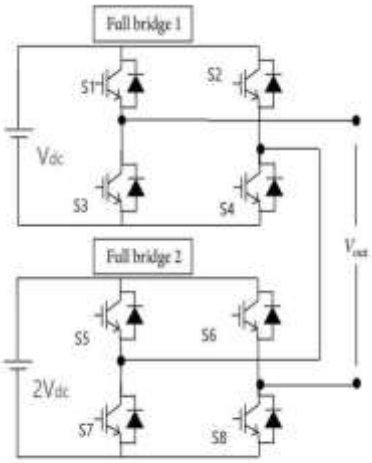

Fig 3.0 Asymmetric cascaded seven level inverter

For the asymmetric seven level inverter to produce the desired stepped output waveform each individual cells are required to oscillate among their respective voltage levels such that when connected in series produce the desired output. For e.g. when the output required at the output required is '+3Vdc' then the 2Vdc cell should generate '+2Vdc' and the 1Vdc cell should generate '+1Vdc' at the output. And if the output required is '+2Vdc' then the 2Vdc cell should generate '+2Vdc' and the 1Vdc cell should generate '0' V. likewise the rest of the output voltages are generated by suitable combinations of the individual cells. Consider the above fig 3.0, for a output voltage of '+3Vdc' the switches (S1,S4) of first H-bridge and switches (S5,S8) of the second h-bridge are turned ON and for the remaining output voltages the switching states are shown in Table 2.0

Table 2.0

Output voltage states	S1	S2	S3	S4	S5	S6	S7	S8
+3Vdc	1	0	0	1	1	0	0	1
+2Vdc	0	0	1	1	1	0	0	1
+1Vdc	1	0	0	1	0	0	1	1
0	0	0	1	1	0	0	1	1
-1Vdc	0	1	1	0	0	0	1	1
-2Vdc	0	0	1	1	0	1	1	0
-3Vdc	0	1	1	0	0	1	1	0

Therefore the required output levels are produced by timely pulses generated from specified control mechanism connected to these switches. There are many control mechanisms developed for multilevel inverters such as Multilevel sinusoidal PWM, Space vector modulation technique, Selective Harmonic Elimination etc. In this paper multicarrier based level shifted Pulse width Modulation (PWM) is employed.

4. CONTROL MECHANISM (or) MODULATION STRATEGY

The control mechanism involves generation of suitable timely switching pulses for the power semiconductor switches to obtain a reduced harmonic output with desired characteristics. Pulse Width Modulation techniques involves the comparison of high frequency carrier signal (usually triangular) with a power frequency reference signal(usually sinusoidal) to generate pulses which substantiate the reference signal characteristics in the form of varied width in pulses. PWM techniques are developed for multilevel converters by increasing the number of carrier signals to suffice with the number of levels of the output voltage. Usually for a 'n' level inverter the number of carrier signals required are 'n-1'.

4.1 CONTROL MECHANISM FOR SYMMETRIC FIVE LEVEL INVERTER

For a five level output voltage four carrier signals are required as shown in Fig.4.0.

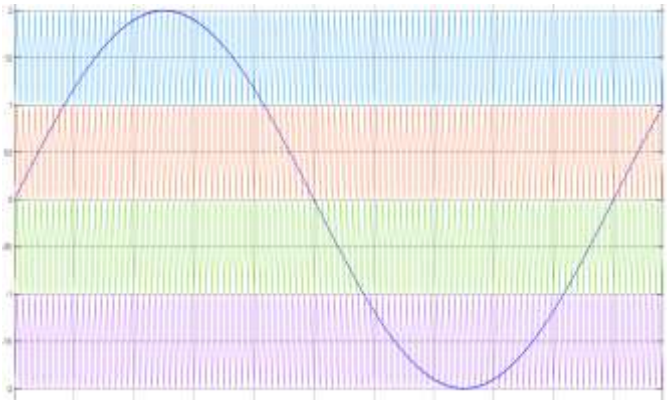

Fig 4.0 Reference(sinusoidal) signal and Carrier(triangular) signals

As shown in the above figure(Fig 4.0), four carrier signals are required to generate a four level output. In MATLAB/Simulink the reference signal is constantly compared with the four carrier signals by relational comparators to obtain four outputs in binary form (either ON or OFF). These signals which are boolean in nature can be subjected to boolean operations if needed to obtain the desired switching pulses for the power switches. For a five level inverter there are eight switches. Consider the fig 2.0, where in for the full bridge the switch pair (S1,S3) cannot be turned ON simultaneously which results in short circuit, likewise the switch pairs (S2,S4),(S5,S7),(S6,S8) are also limited from turning ON simultaneously which makes these switches complementary i.e. turning ON one of this switches needs the other switch to be turned OFF. This property eases the design of control strategy by deign the switching mechanism for one switch of one leg and the switch's gate circuitry can be obtained by connecting a NOT gate to the earlier switch's gate circuitry. The gate circuitry for the five level inverter is shown in the fig5.0. In the fig 5.0 the carrier signals are generated by triangular wave generators and the reference signal is generated by sinusoidal signal generator and the outputs are compared using relational comaparators. These relational comparators' outputs are directly connected to switches S1,S2,S3,S4,S5,S6,S7,S8 of the Fig 2.0.

The triangular signal generators shown in the fig 5.0 are in accordance with the adjacent placing of carrier waves as shown in the fig 4.0, and the switches' nomenclature is in accordance with the switches in that of fig 2.0. The above circuit after connecting with the designated switches produces a Five level output voltage.

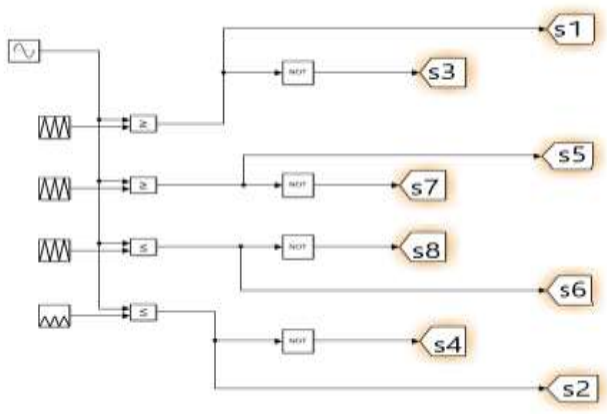

Fig 5.0 Gate circuitry for five level inverter

4.2 CONTROL MECHANISM FOR ASYMMETRIC SEVEN LEVEL INVERTER

From the above synopsis it can be deduced that for a seven level output, six carrier signals are required as shown in the fig 6.0.

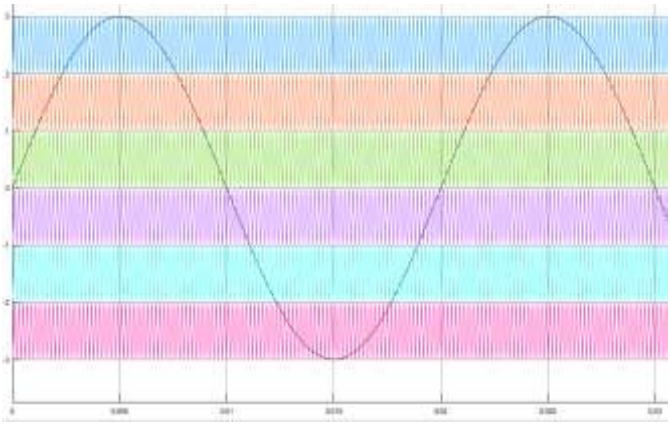

Fig 6.0 Reference(sinusoidal) and Carrier(triangular) signal

In MATLAB/Simulink the reference signal is constantly compared with the six carrier signals by relational comparators to obtain six outputs in binary form (either ON or OFF). These signals which are boolean in nature can be subjected to boolean operations if needed to obtain the desired switching pulses for the power switches. Since asymmetric seven level inverter also consists of H-bridges, there exists complementary switch pair. Unlike the symmetric topology where the relational comparators` output suffice with number of switches, in seven level inverter the relational comparators' output are subjected to XOR gate boolean operation as shown in Fig 7.0

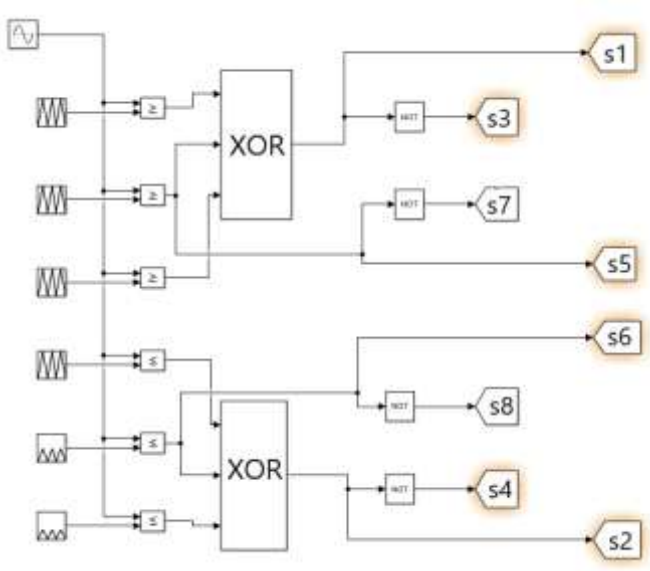

Fig 7.0 Gate circuitry for asymmetric seven level inverter

The gate circuitry for the five level inverter is shown in the fig7.0. In the fig 7.0 the carrier signals are generated by triangular wave generators and the reference signal is generated by sinusoidal signal generator and the outputs are compared using relational comaparators and the final outputs are connected to switches S1,S2,S3,S4,S5,S6,S7,S8 in the topology shown in Fig 3.0.The triangular signal generators shown in the above fig 7.0 are in accordance with the adjacent placing of carrier waves as shown in the fig 6.0, and the switches' nomenclature is in accordance with the switches in that of fig 3.0. The above circuit after connecting with the designated switches produces a seven level output voltage.

5. SIMULATION RESULTS

The single phase inverter is developed for three phase and is fed to a three phase induction motor. Unlike diode clamped and flying capacitor where one Dc source is sufficient for single phase as well as three phase, in cascaded H-bridge type three phase is developed by connecting three single phase inverters to make a three phase four wire system

5.1 SIMULATION RESULTS OF SYMMETRIC CASCADED FIVE LEVEL INVERTER: A symmetric five level inverter is simulated in simulink/MATLAB with the control circuitry shown in the fig 5.0. The input DC source magnitudes are adjusted so as to match the ratings of the three phase induction motor, and the induction motor ratings are 5.4HP (4KW), 400V, 50Hz, 1430 rpm. The simulation results are as follows **fig8.1** three phase output **fig 8.2** FFT analysis of five level output, **fig 8.3** stator phase current, **fig8.4** speed characteristics, **fig 8.5** torque characteristics

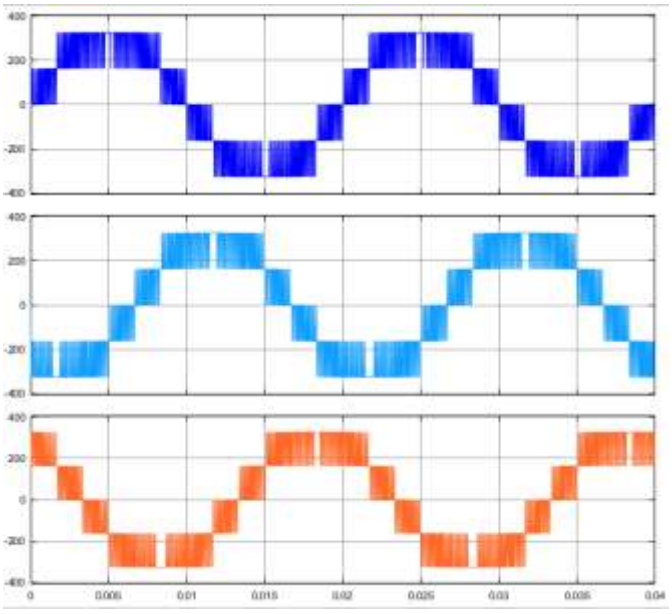

Fig8.1 Three phase five level output

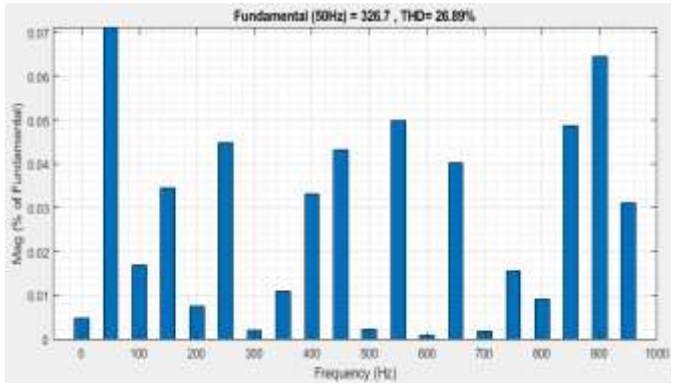

Fig 8.2 FFT analysis of five level output voltage

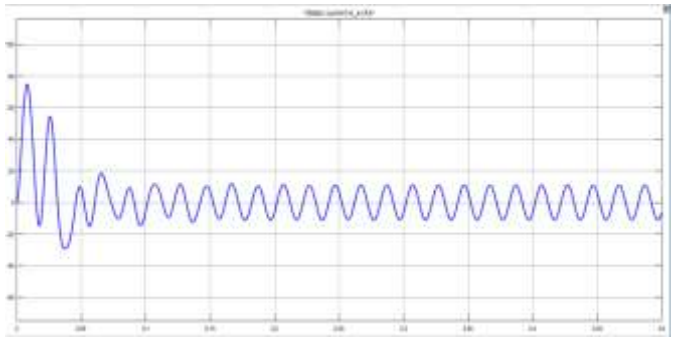

Fig 8.3 Stator phase current

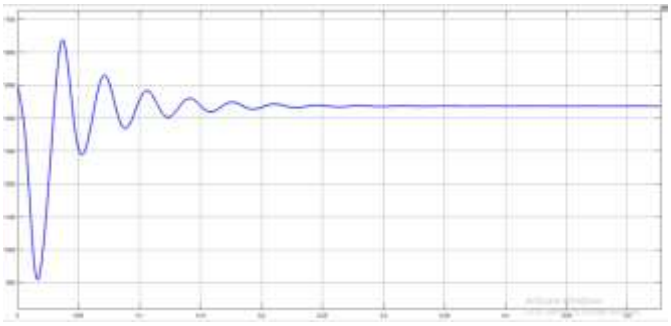

Fig 8.4 Speed characteristics

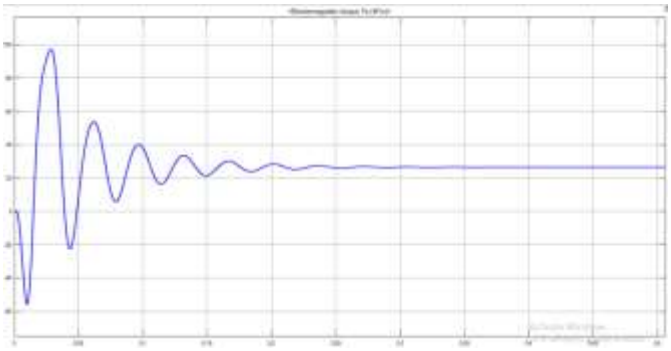

Fig 8.5 Torque characteristics

5.2 SIMULATION RESULTS OF ASYMMETRIC CASCADED SEVEN LEVEL INVERTER: An Asymmetric seven level inverter is simulated in simulink/MATLAB with the control circuitry shown in the fig 7.0. The input DC source with less magnitude adjusted so as to match with ratings of three phase induction motor and the induction motor ratings are 5.4HP (4KW), 400V, 50Hz, 1430 rpm. The simulation results are as follows **fig 9.1** three phase output **fig 9.2** FFT analysis of seven level output, **fig 9.3** stator phase current, **fig9.4** speed characteristics, **fig 9.5** torque characteristics.,

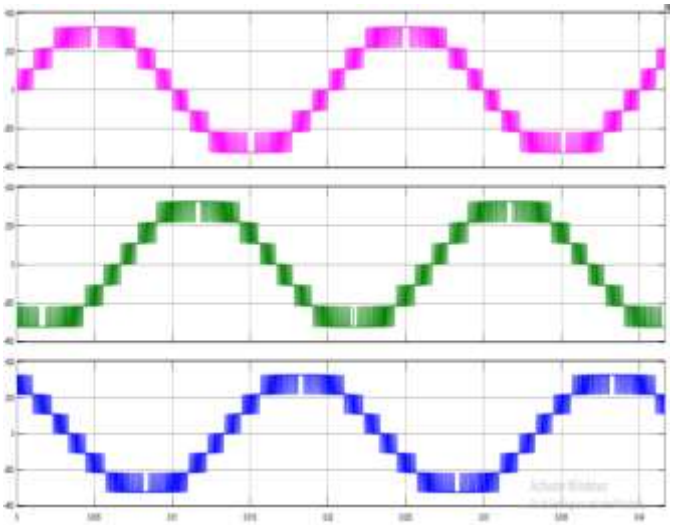

Fig 9.1 Three phase seven level output

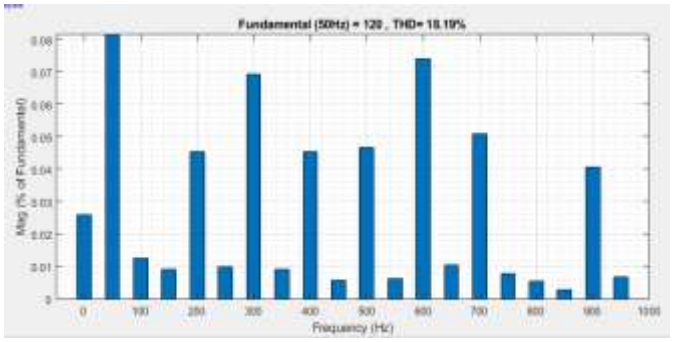

Fig 9.2 FFT analysis of seven level output voltage

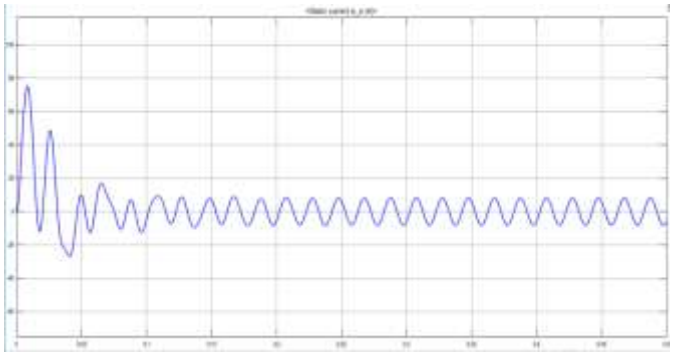

Fig 9.3 Stator phase current

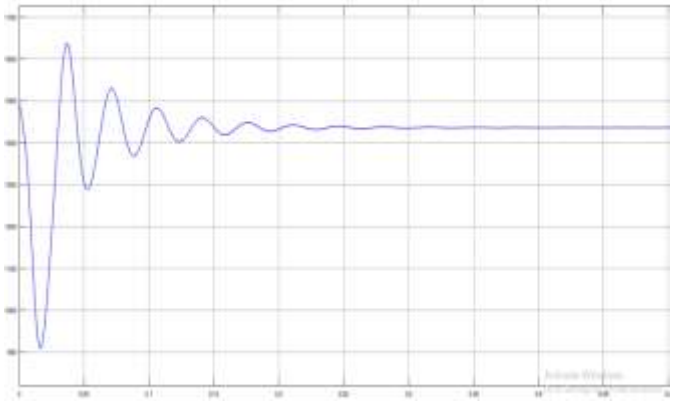

Fig 9.4 Speed characteristics

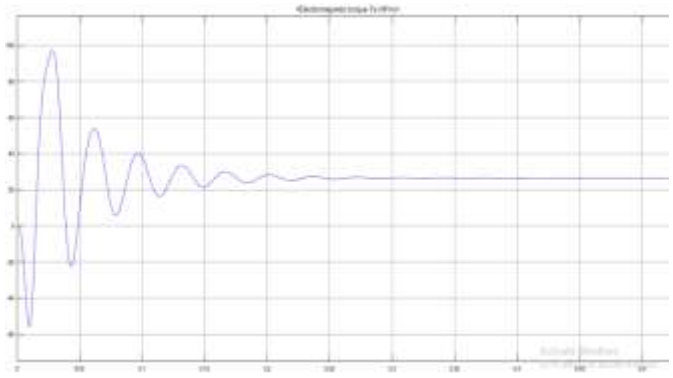

Fig 9.5 Torque characteristics

6. COMPARISON OF SYMMETRIC FIVE LEVEL INVERTER AND ASYMMETRIC SEVEN LEVEL INVERTER

Table 3

Parameter	Symmetric Five level	Asymmetric Seven level
Number of output levels	5	7
Number of power semiconductor switches	8	8
Number of DC sources	2	2
Number of H-bridges	2	2
THD(Total Harmonic Distortion)	26.18%	18.19%
Ratings of power switches(in practical realization)	All switches are of same rated voltage	Switches corresponding to one H-bridge are of same rated voltage and are different from other H-bridge switches

It can be observed from the above comparison table 3,that the harmonic content is **less in seven level inverter than in five level inverter.**

Each cell in an asymmetric multilevel inverter has unique characteristics accounting to the unequal DC sources and same voltage output cannot be produced by mere exchanging of control strategy among two cells unlike Symmetric topology, which also signifies the point that all the switches in a asymmetric seven level inverter are not subjected to same **OFF** state voltages as in Five level inverter.

The control circuit/gate driver circuit in a symmetric cascaded MLI requires less computations without much binary operations, whereas in an asymmetric cascaded MLI the control circuitry is more complex and gets more complicated with more boolean operations with the increase in output levels. This becomes a limitation for the asymmetrical topology as levels increases which makes the practical realization less feasible.

7. CONCLUSIONS

The simulink/MATLAB models for symmetric cascaded five level inverter and asymmetric cascaded seven level inverter are developed using Level Shifted Carrier based Pulse Width Modulation technique(In Phase disposition).

From the performance analysis (THD) it can be observed that the voltage spectrum of asymmetric cascaded seven level inverter is better compared to the voltage spectrum of symmetric cascaded five level inverter.

For the seven level inverter the motor characteristics speed, torque attained a fairly constant value and the stator and rotor current characteristics attained a stable sinusoidal (non deviating) at nearly 0.2sec which is very small and less than the value attained by five level inverter. The asymmetric cascaded multilevel inverter is found to have better characteristics for a two bridge setup.

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