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Review of Leakage Power Recovery Methodologies in VLSI Design

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Abstract - *This paper reviews different techniques and concepts related to recovery of Leakage power in lower nanometer technologies. As the technology scale decreases, leakage power is putting same impact when compared with total power dissipation. Exponential growth rate of leakage is due to the trends like scaling of thickness of gate oxide, channel length, dopants profiles which are combined with transistors in a chip. Every VLSI design needs to be corrected during physical implantation stages to avoid design rule constraints violations. Engineering Change Order (ECO) phase involves such corrections like introducing spare cells in the layout. But in stand-by mode, these spare or ECO cells lead to a large sub-threshold leakage power. One of the techniques uses state depended leakage power table by assigning optimal standby to each spare cell's inputs to mitigate leakage power and its effects. Leakage recovery and optimization of the design is possible up to some extent.*

Key Words: Engineering Change Order (ECO), State dependent leakage power, Total negative slack (TNS), Subthreshold leakage power.

1. INTRODUCTION

The major performance parameter in the design modules of Wireless communication equipment, networking modules is minimization of power. On the other side higher performance, good integration, dynamic power dissipations are some of the parameters which drives scaling of CMOS devices. As the technology shrinks the leakage current or leakage power is dramatically increasing in comparison with dynamic power dissipation. The main fact behind increment in static power dissipation is Leakage power which involves many contributors towards it, gates oxides tunneling effect of leakage, bands to bands tunneling (BTBT) effect of leakage and subthreshold effect of leakage [1]. The differences of devices in electrical and geometry parameters like variation in gate width and in its length dramatically affect the subthreshold leakage current [2]. Certain leakage elements include Drains Induces Barriers Lowering (DIBL) and Gates Induce Drain Leakages (GIDL) etc., [3]. Most significant sources of leakage for 65 nm and below scaled CMOS devices are: leakages at gate site, subthreshold leakages and leakage due to BTBT at reversed biased junction. Reduction of threshold value of voltages leads to increment in subthreshold current which is allowed to retain transistor in ON state with the help of dropping voltage. Due to the scaling of thickness of gate oxide, the current density of the gate leakage is increasing, resulting in rising tunneling current. The magnitude value of every leakage factor depends on the technologies involved for the operation. Self-Controlled voltage levels (SVL) techniques can be used to minimize effect of leakage [4].

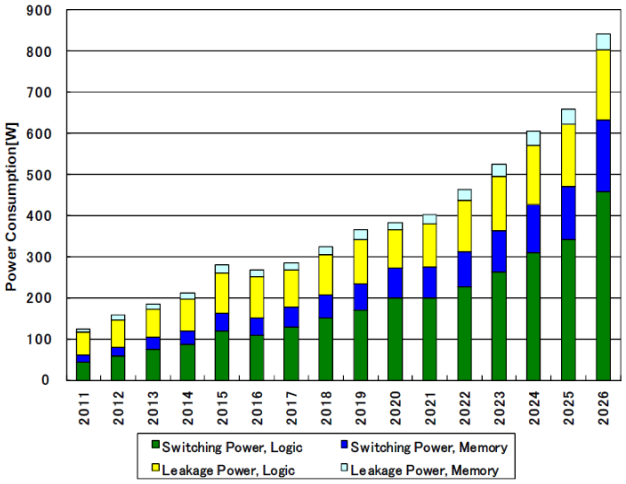

Fig -1: Power Consumption Trends (from ITRS) [6]

Usage of the dielectric gate having higher K value, however helps to minimize the risk of leakages of gate oxide and when higher K valued dielectric element is used in design, main characteristic feature like mobility of channel degrades which leads to reduction in efficiency. To boost output Silicon-Germanium layer was used to strains Silicon to address minimized carriers' mobility. This leads to the sub-threshold leakage as well as BTBT leakage current to increase [5]. Reverse-based BTBT leakage is rising due to changes in the depletion width of the junction needed to absorb short channelled effect (SCE) of transistors. When technologies scale down, the ratio of power dissipation due to leakage to power dissipation in total increases with each node steadily as seen in Fig.1. Leakage is an undesirable by-product and drastically affects the devices' running time thereby making these products non-competitive. Therefore, mitigating leakage is absolutely necessary, wherever possible. When the leakage becomes increasingly relevant with feature size reduction in overall power consumption, the purpose of such implementations is too reach timings along with its minimum possible leakages. There are various models and design approaches to minimize overalls power

dissipation, but the challenges of achieving the optimum library cell mixing for the lowest power at that speed remains as it is.

2. Spare cell based VCO

Design leakage has its own importance towards data path combinational logic, sequential elements, memory block and stand by circuit spare cell or ECO cell connection. Spare cells are nothing but redundant cells. They are also known as extra cells allocated as backup cells. for the implementation of any ECOs that may be essential part in the design. Some of the Spare cells will be inactive stage and some cells may be connected selectively to the components while rerouting of ICs. This mechanism is referred to ECO and here ECO cells refers to spare cells. Various configurations of HVTs cells, SVTs cells and LVTs cells would be poured into the system center as extra cells depending on the efficiency of the system and switching operation involved. Not only do spare cells occupy more chip areas that have a huge effect on gain, but they are also responsible for further leakage power. Spare cells contribute 5-20 per cent of the overall number of cells in an IC [7]. Although the subsequent architecture changes will not use all extra cells, there is a large amount of power leakage over the chip's lifespan due to cells which are not part of the logic. Unused these spare cell inputs are attached to high voltage (VDD) and low voltage (VSS) supply lines in conventional design flows, which is known as constant injection method, that can draw leakage current or static current [8]. Yet the approaches of still connecting redundant cell inputs to grounds or high voltage won't ensure low leakage. Functional ECO's are concerned with making rational interface improvements. A functional ECO's key goal is to handle RTL improvements with no significant disruption to the converged layout. Nonfunctional ECOs manage modifications concerning the quality of the signal, design rules verification or process like routing. The count of spare cells as well as its types depend on module design complexity and its functionality. But it is preferable to utilize universals gates in the design to achieve most of the functionality. BUF, INV, NOR and NAND are the most useful spare cells. XOR like complex gates are rarely used [9].

3. State Depended Leakage Power

The power leakage dissipation of the logic gates is related to various states of gate inputs. This is known as state depended leakages power consumption of the logic gates. For any kind of CMOS logic having N inputs, there could be 2^N states. For each state of gate, the leakages powers consumption is calculated with the usage of circuits simulation models. It is stored in a proper format that the EDA tools may use to obtain state-dependent leakage power. Each library file will contain cell features. The EDA tools is used to calculate the leakage power dissipation to optimize the functional paths. Total value of leakage power will be calculated as addition of all such conditions of the model multiplied with its occurrence probability.

4. Techniques Used

Let's take example of AND gate in library file consisting of two input pins A, B. Input to this gate have 4 different combinations (D1, D2, D3, D4). These combinational inputs will have its own state dependent leakage values. Table 1 summarizes state dependent leakage power of AND gate. According to the conventional method, if X and Y input pins of the given AND gate are connected to ground or low voltage, D4 will be verified as true and the corresponding leakage value will be Val 4 and the probability that certain conditions D1, D2 and D3 will occur would be zero. Leakage calculation will be easy now because few of the term values are zero. Yet leakage factor Val 4 need not be the table's lowest possible value. That is the problem with the conventional method of linking all inputs of spare cells to ground.

Table -1: State Dependent Leakage Power of two input AND gate [6]

Input Conditions	Leakage Value
D1 (X, Y)	Val 1
D2 (X!, Y)	Val 2
D3 (X, Y!)	Val 3
D4 (!X, !Y)	Val 4

Therefore, one strategy is implemented in which the state-dependent method of minimizing the leakage is used to idle spare cells where maximum state is applied to inputs of gate which will ensure the lowest leakage [6]. First minimum leakage value Valmin will be found for the spare cells or gates in the proposed algorithm or flow, and corresponding input state Dmin will be found from the.lib modules and tied the inputs of spare cell based on its state. From this, it will be magnified to many instances present in the design and the analysis will be done based on the data. This approach is used to find optimal state giving minimal leakages value from state dependent leakage power table from the .lib files and giving links to inputs accordingly. The algorithm or flow is written with the use of commands of tcl which will be helpful to do operations in placement as well as routing stages of design flow.

5. Results and Discussion

This algorithm has been used to connect inputs of spare cells to an optimized state that guarantees minimum standby leakage on the architecture of Lowest Voltage Differential Signaling. Here multi-threshold libraries of Synopsys SAED

32 nm, and 65 nm, 45 nm and 40 nm Synopsys Module Wares Multi-thresholds libraries having of HVTs cells, SVTs cells & LVTs cells are used. This synopsis tool will help to obtain gate leveled netlist. First few bunch of design implementation results of layout are shown in Table 2 in which threshold (Vt) cells are varied across multiple libraries of various technologies to notice the variation in leakage. Based on simulation data 7 to 13% of whole design module cells as redundant cells in these design layouts. The majority of spare cells are NOR, INV, AND, OR, BUF and NAND gates. Scannable flops are added to each clock group. The combination of LVT cells, SVT cells and HVT cells shall be retained in Table 2 in compliance with the timing specifications and the LVT spare cells count shall be reduced to 20% of the total redundant cells count.

Table -2: Leakage Recovery using Standalone Vt cell across Different Technology [6]

Technology (Vt-cell)	Total Leakage of the Design (uW)	Leakages of spare cell with proposed Flow (nW)	Leakages of spare cell in the design (%)	Reduction of Leakage in the total design (%)
Lvt65nm	1.204	40.283	3.40656	1.73032
Lvt45nm	47.422	1510.1	3.22739	1.32322
Lvt40nm	2.970	151.559	5.23113	2.35246
Lvt32nm	578.984	22198	3.8962	1.53141
Svt65nm	305601	10.597	3.52945	1.72021
Svt45nm	21.488	774.427	3.65875	1.40052
Svt40nm	1.191	36.356	3.08741	1.08128
Svt32nm	87.164	3332	3.83862	0 .43799
Hvt65nm	23454	0.69151	2.99428	1.48111
Hvt45nm	6.508	250.049	3.88702	1.09577
Hvt40nm	192856	6.987	3.6519	0.71677
Hvt32nm	26.196	793.798	3.04	0.35173

Usage of HVT cells will primarily reduce the leakages capacity by retaining design time as well as total negatives slacks (TNS). Tcl-script language-based algorithm is used to allocate optimal states to input of spare cells extracted from leakage tables after spreading ECO cells into the structure at the process of placement point. Likewise, Inputs of remaining spare cell structure are connected to ground. Synopsis prime time tool will give implementation results on considering various parameters like temperature, voltage, fanout, sigma value, technology etc. Now finally at this stage we haves used the Synopsis Prime Time signoffs powers tool to evaluate the leakage capacity of the system and contribution of spare cells against product leakage in all model layouts. With the proposed flow, around 48% to 30% of the recovery of leakage in redundant cells is seen and it is consistent among multiple VTs cells.

6. CONCLUSION

New state depended tables of leakage are based on giving proper links to ideal redundant cell inputs that ensure minimal leakage capacity in correspondence to current fixed insertion system where all the gate inputs are connected to ground or high voltage. Measuring leakage of standard cells has been tested much earlier by using state dependent table of leakage method. The proposed system can be examined on post-positioned layout designs using 65nm and lower technology, and tests after process of routing reveal that significant reduction in the leakage power of redundant cells from 48 to 30% is seen and overall standby IC leakage is also comparatively reduced in the range of 1.7% to 0.7%. The proposed approach can easily be applied to new designs, with minute modifications in design flow.

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