DESIGN AND ANALYSIS OF ALL OPTICAL PHOTONIC AND, NOR, NAND AND XNOR

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Abstract:

In this paper we proposed 2-D photonic crystals to design AND, NOR, NAND and XNOR. The proposed device is formed by the combinational of line defects and square cavity. The performance of the device is anazaled using 2-D finite difference time domain (FDTD) method. The size of designed wafer is 5.4μm×8.4μm. The device has lattice constant, refractive index and rod radius of 0.6, 3.46 and 0.20 respectively. The contract ratio of all optical logic gate for AND, NOR, NAND, and XNOR are 25.037, 9.090, 11.592 and 7.811. The proposed structure is highly compact and suitable for photonic integrated circuits (PIC).

Keywords: Photonic Crystals; Beam-Interference; Logic gates of NOR, AND, NAND and XNOR; T-shaped waveguides; OptiFDTD (finite difference time domain) method.

Introduction:

At recent years, all optical logic gates have received much interest because of their wide applications in photonic networks, optical communication systems and optical computing systems [1-3]. Photonic crystals are more popular due to it takes less time. In order to construct the optical routers, all optical signal processing devices are needed. until now, various optical logic gates have been proposed. In future all optical networks have some advantages, such as low power consumption and high speed [4-11]. Now the technology of 20th century was undoubtedly electronics, the 21th century is predicted to become the century of photonics, it is the advancement of electronics. The main difference between the two is that, in photonics the logic gates are most important because each and every components and devices are designed based on logic gates and whereas in electronics, the Digital Logic Circuits are based on logic gates. [12]. All optical logic gates are key elements in optical signal processing such adderessing, switching, header recognition, data encoding and decryption. All optical logical gates provide high performance in optical networks.

In order to design the logic gates with simple structure i.e., ultracompact size, low power and high-speed we choose photonic crystals [17-19]. In photonic crystal optical processing electron is replaced by photon so high-speed devices can be achieved. Due to these photonic crystals are used for high speed communication. A lot of research works have been alone in the field to realize and optimize the PC's logic gates. Some of them are based on multi-mode interference (MMI) [13-14], photonic crystal ring resonator (PCRR) [15-16], Y-shaped and t-shaped waveguides. Among all of these T-shaped waveguides provides high bit rate we use T-shaped wave guides.

In recent years, all optical logic gates have wide range of applications in real time optical processing and information communication because all optical signal, processing can handle large bandwidth signal. These optical logic gates are expected to be main supporting techniques in future all optical info networks various technologies and materials have been introduced to realize all optical logic gates including optical Fibers, semiconductor optical amplifiers (SOA) [20-21] and photonic crystals but most of these works suffer from limitations such a big size, low speed, high noise and difficult to perform chip scale integration when compared to photonic crystals.

In this paper, we have proposed the design of all optical logic gats based on two dimensional photonic crystals composed of T-shaped lattice of air holes in si. Till now many logic gates designs have been proposed which consist of si rods in air but those designs are not pratical from the point of view of sustainability and fabrication. Photonic crystal composed of air holes in silicon is a more pratical structure and has been used in the design of optical logic gates and nano photonic devices

Design or Structure analysis of all optical logic gates:

A two-dimensional (2D) PhC is proposed with an array of Si rods in air background arranged in two T-type lattices, and the refractive index of each rod is 3.46. The radius of each Si rod is 0.2a, where a is the lattice constant of value 600nm. The size of wafer is 5.4 µm×8.4 µm. At the junction (Rj) size of radius 0.4a, reflecting rod Rf1 of the radius 0.2a is placed, and reflecting rod Rf2 also be placed so that light signal from the reference port will propagate towards the output port. In there we want to be reduced back reflection we used the reflecting rod and junctions. Waveguides are created by deleting the rods. In there we want to design the all optical logic gates they are AND, NOR, NAND and XNOR here we want to be used the two-input port, one reference port and one output port. At there we use the reference port should be denoted as 'R', input ports should be represented as the 'A' and 'B' where A is the first input port and B is second input port. The proposed design will be shown in below fig.1
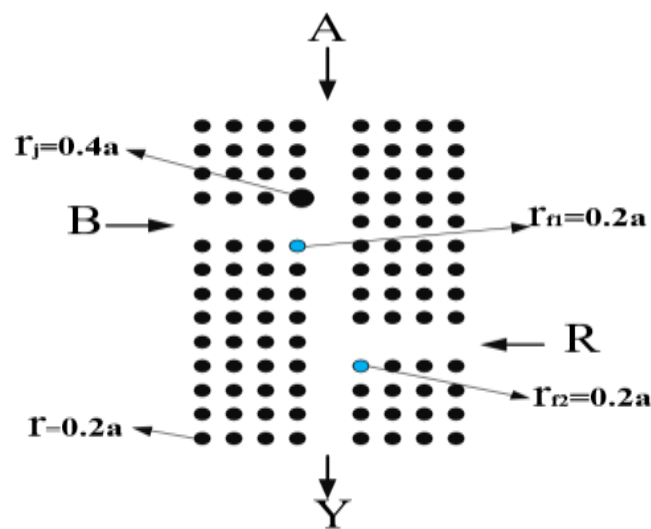

Fig. 1: Proposed all-optical NOR, NAND and XNOR structure

The proposed structure of all optical logic gates is NOR, NAND and XNOR is based on the principle of beam interference. Beam interference can be two types they are constructive or destructive that can base on the phase differences and path differences. When the phase difference of two incoming signals is 180^0 and even integral multiple of path difference creates Destructive Interference and vice versa. When phase difference of two incoming signals is 0^0 and even integral multiple of path difference creates Constructive Interference and vice versa. The optimized device can give the contract ratio for NOR gate is 9.090, NAND gate is 11.592 and XNOR gate is 7.811.

In there we should be want be done with same simulation for the AND logic gate will be change with the inputs and reference ports will be change with the same measurements. By there we will be takes the input port A can be taken as the reference port, input port B can be taken as the input port A, reference port can be taken as the input port B. Remaining all the properties should same as the fig.1 The optimized device of AND gate can give the contract ratio should be 25.037. The proposed structure should be done in below Fig.2
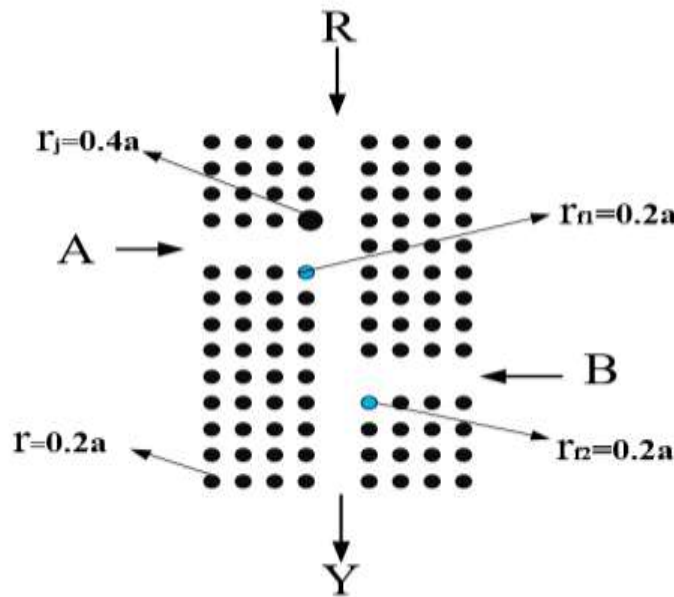

Fig. 2: Proposed all-optical AND structure

Simulation results:

AND gate results:

Case 1:

When both of the input ports (port A and port B) have been excited phase angle Ø=0° with logic 0, and only the reference port R having phase angle Ø=180°, have been excited then logic 0 is obtained at the output port Y.

Case 2:

When the input port A has phase angle ∅=0° with logic 0 and input port B have been excited phase angle ∅=180° with logic 1, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.
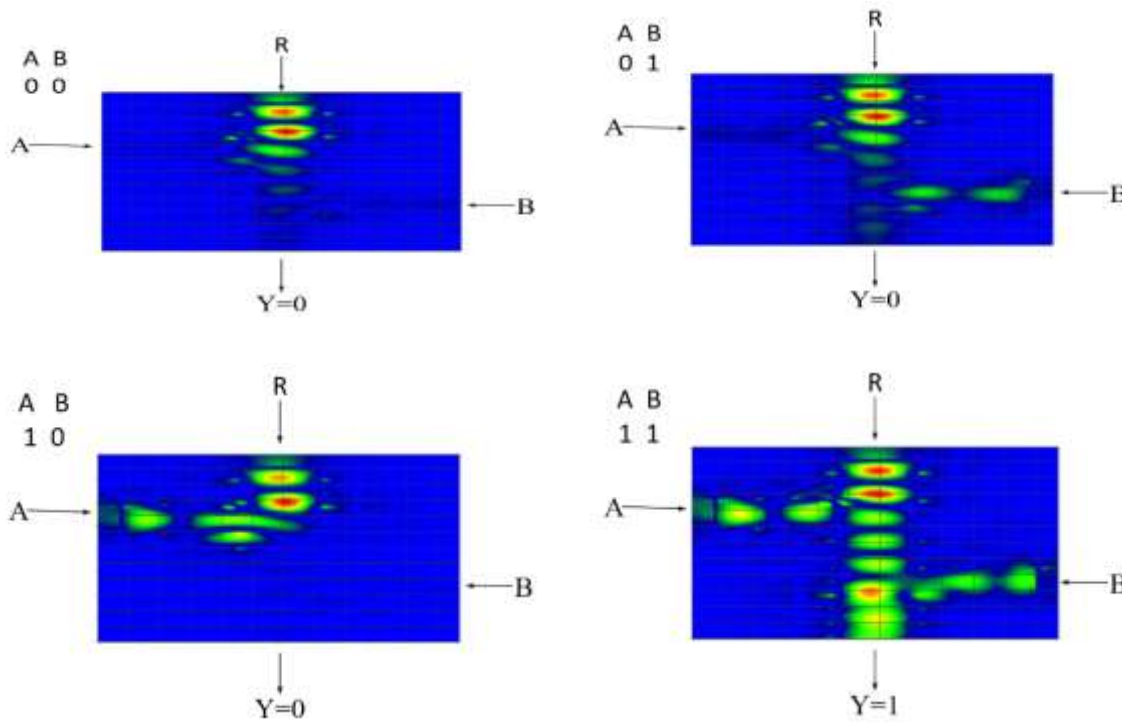
Case 3:

When the input port A has phase angle ∅=180° with logic 01and input port B have been excited phase angle ∅=0° with logic 0, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 4:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 1, and only the reference port R having phase angle ∅=180°, have been excited then logic 1 is obtained at the output port Y.
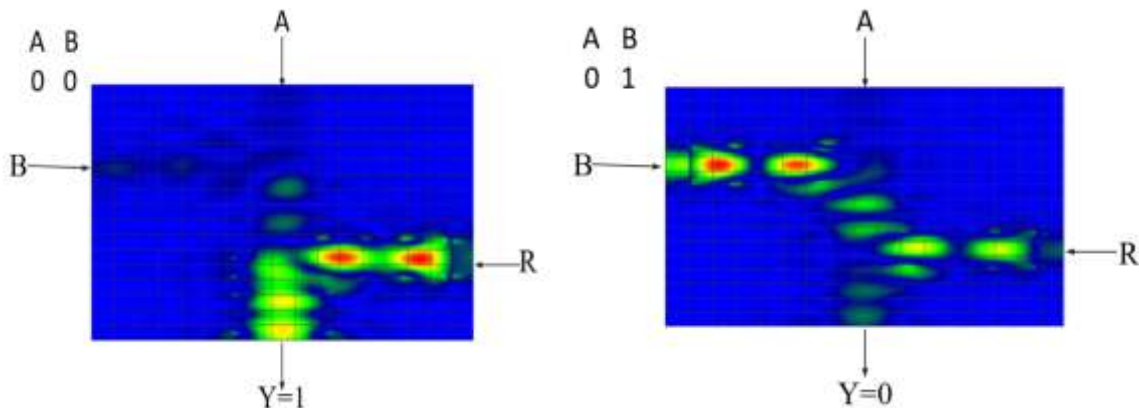

Fig.3: Output results for AND gate with different inputs (00, 01, 10 and 11)

Input A		Input B		Reference R		Output Y	
logic	Phase angle	logic	Phase angle	logic	Phase angle	Logic	power
0	0°	0	0°	1	180°	0	0.059
0	0°	1	180°	1	180°	0	0.270

1	180°	0	0°	1	180°	0	0.005
1	0°	1	0°	1	180°	1	1.595

Table 1: Truth table for AND logic gate

NOR gate results:

Case 1:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 0, and only the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 2:

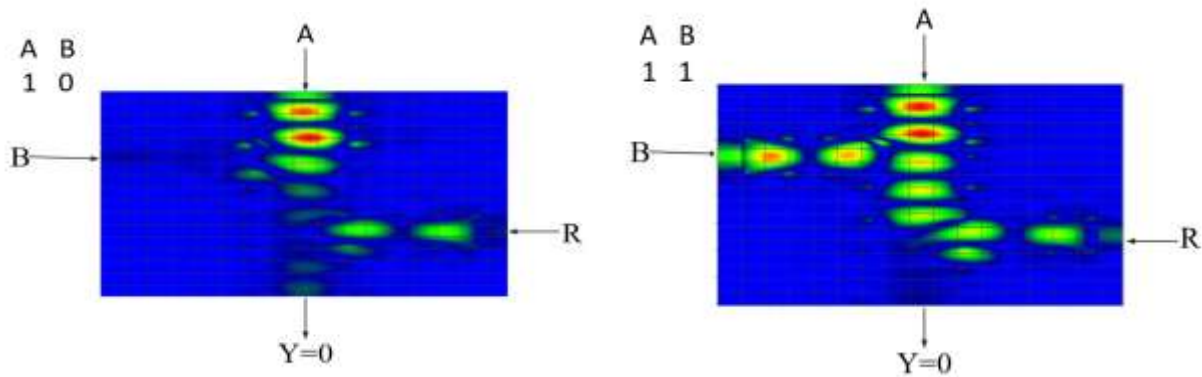When the input port A has phase angle ∅=0° with logic 0 and input port B have been excited phase angle ∅=180° with logic 1, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 3:

When the input port A has phase angle ∅=180° with logic 01and input port B have been excited phase angle ∅=0° with logic 0, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 4:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 1, and only the reference port R having phase angle ∅=180°, have been excited then logic 1 is obtained at the output port Y.

Fig.4: Output results for NOR gate with different inputs (00, 01, 10 and 11)

Input A		Input B		Reference R		Output Y	
logic	Phase angle	logic	Phase angle	logic	Phase angle	Logic	power
0	0°	0	0°	1	180°	1	0.584
0	0°	1	0°	1	180°	0	0.264
1	180°	0	0°	1	180°	0	0.270
1	180°	1	0°	1	180°	0	0.072

Table 2: Truth table for NOR logic gate

NAND gate results:

Case 1:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 0, and only the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 2:

When the input port A has phase angle ∅=0° with logic 0 and input port B have been excited phase angle ∅=180° with logic 1, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 3:

When the input port A has phase angle ∅=180° with logic 01and input port B have been excited phase angle ∅=0° with logic 0, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.
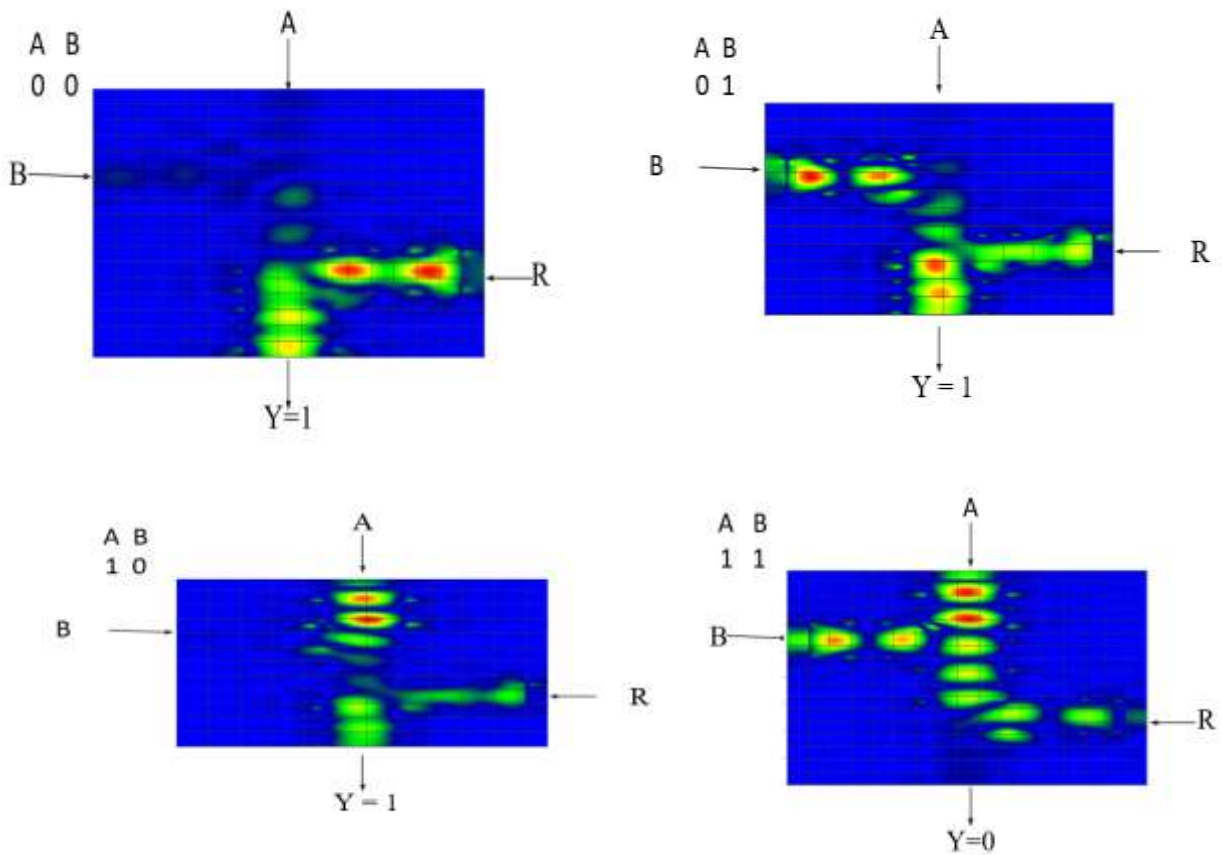
Case 4:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 1, and only the reference port R having phase angle ∅=180°, have been excited then logic 1 is obtained at the output port Y.

Fig.5: Output results for NAND gate with different inputs (00, 01, 10 and 11)

Input A		Input B		Reference R		Output Y	
logic	Phase angle	logic	Phase angle	Logic	Phase angle	Logic	power
0	0°	0	0°	1	180°	1	0.584
0	0°	1	0°	1	0°	1	1.039
1	180°	0	0°	1	0°	1	1.018
1	180°	1	0°	1	180°	0	0.072

Table 3: Truth table for NAND logic gate

XNOR gate results:

Case 1:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 0, and only the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 2:

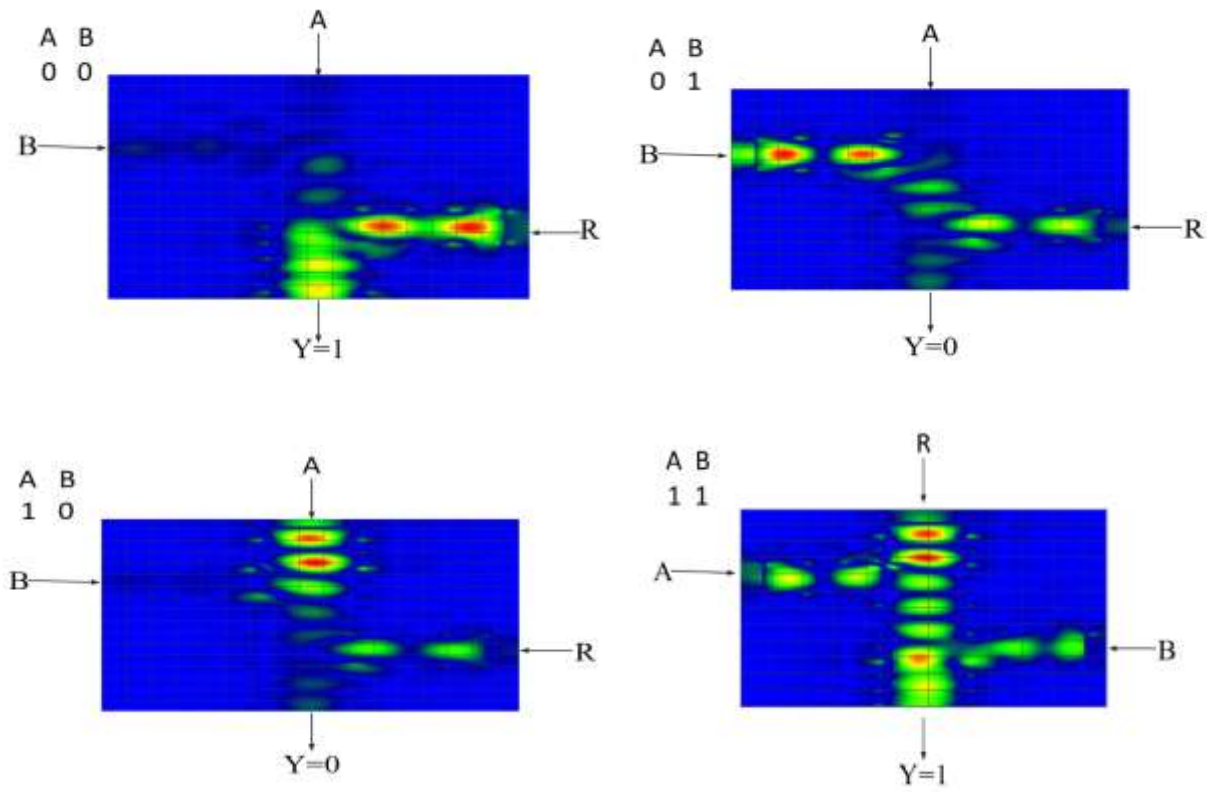When the input port A has phase angle ∅=0° with logic 0 and input port B have been excited phase angle ∅=180° with logic 1, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 3:

When the input port A has phase angle ∅=180° with logic 01and input port B have been excited phase angle ∅=0° with logic 0, and the reference port R having phase angle ∅=180°, have been excited then logic 0 is obtained at the output port Y.

Case 4:

When both of the input ports (port A and port B) have been excited phase angle ∅=0° with logic 1, and only the reference port R having phase angle ∅=180°, have been excited then logic 1 is obtained at the output port Y.

Fig.6: Output results for XNOR gate with different inputs (00, 01, 10 and 11)

| Input A		Input B		Reference R		Output Y	
logic	Phase angle	logic	Phase angle	logic	Phase angle	Logic	power
0	0°	0	0°	1	180°	1	0.584
0	0°	1	0°	1	180°	0	0.264
1	180°	0	0°	1	180°	0	0.270
1	180°	1	0°	1	0°	1	1.595

Table 4: Truth table for XNOR logic gate

The operation all optical logic gates of AND, NOR, NAND and XNOR done with different waveguides and rod radius. The graphs are drawn with different waveguides vs contract ratio and different rod radius vs contract ratio also be done the graphs. The wavelengths are taken from 3.40 to 3.50 in their we can observe the better results was 3.46 and the rod radius were taken 0.18a to 0.22a at these values we can be observe the best result is 0.20a radius with refractive index is 3.46 the graphs are shown in below Fig.7
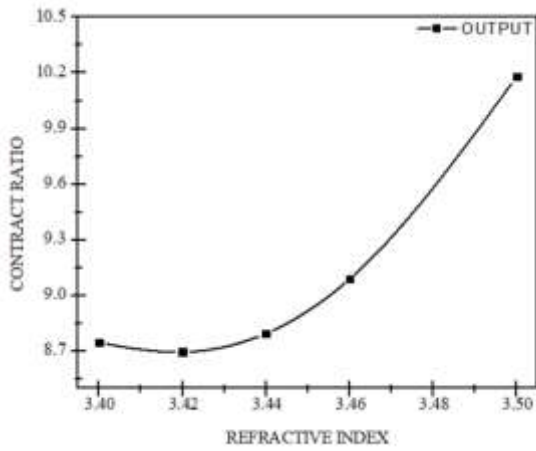
The formula of the contract ratio is CR =10log (P1\ P0), Where P1 is output power of the logic 1, P0 is the output power of the logic 0
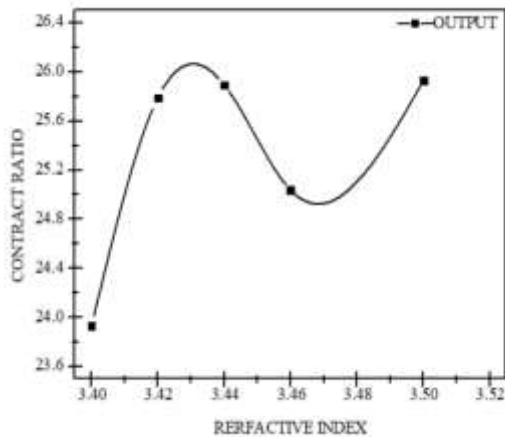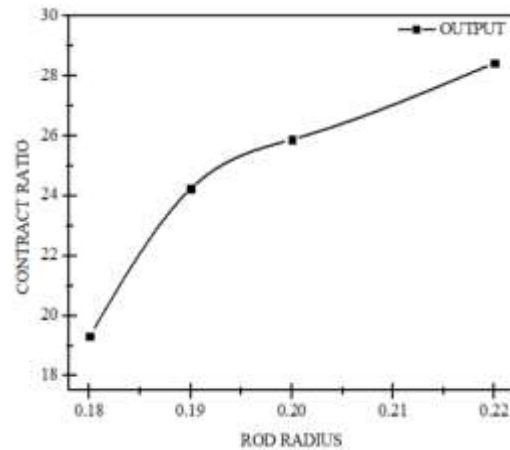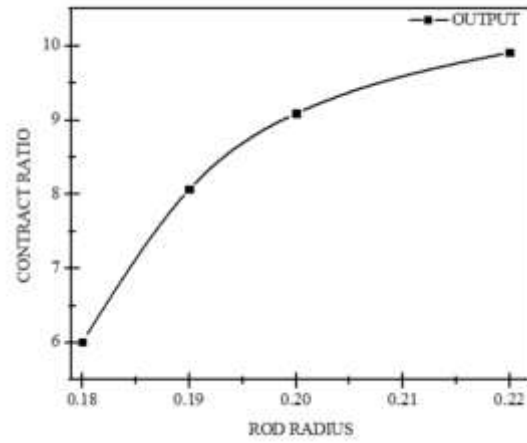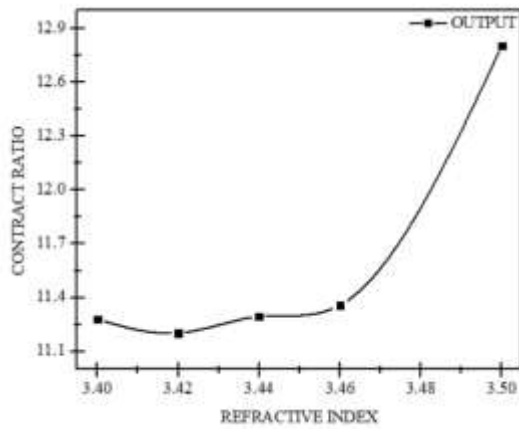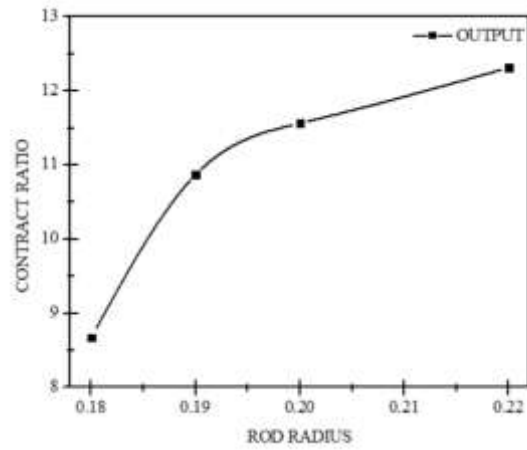

1(a)   1(b)
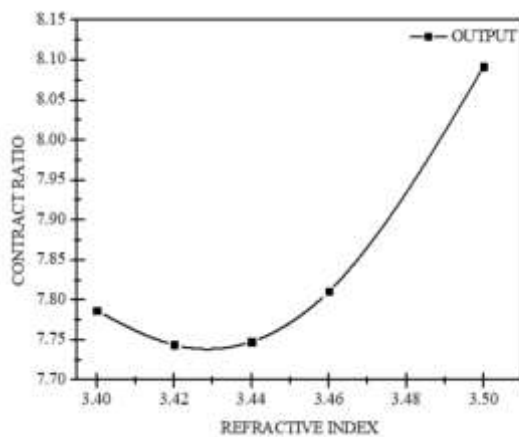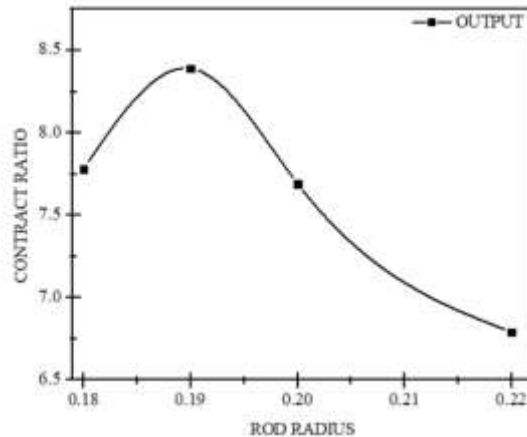
2(a)

2(b)

3(a)

3(b)

4(a)

4(b)

Fig.7 Contract ratio for all optical logic gates AND(1), NOR(2), NAND(3) and XNOR(4) for different refractive index(a) and rod radius(b)

Conclusion:

In this paper, we design the AND, NOR, NAND and XNOR are can be T-shaped waveguides. In their we got reflecting and junction rods at the place of input ports and has high contract ratio. By applying the principle of the beam interference, at that time changing the phase angles in input ports. The structure was designed and verified by using the OptiFDTD (finite difference time domain) method. The contract ratio for the all optical logic gates (AND, NOR, NAND and XNOR) is 25.037, 9.090, 11.592 and 7.811. These are helps for the high-speed operational systems and optical networks.

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