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Space Vector Modulation based Control Technique for Shunt Active Power Filter

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Abstract - *This paper presents the method of elimination of harmonics by using the reference frame theory applied on Voltage Source Converter (VSC) of a Shunt Active Power Filter (SAPF). As harmonics play a vital role in occurrences of faults and disturbances in the system, the method which is discussed in this paper shows superior results due to the uniqueness in construction than the conventional Voltage Source Converters. As the conventional voltage – current controllers have their own disadvantages, in this method the P-I controller is used to obtain some rigorous control over the system. Also as the conventional a-b-c stationary frame is not more controllable hence is replaced by the d-q-0 rotating frame. The method is basically based on Pulse Width Modulation technique in which the Space Vector Modulation (SVM) is used which having certain advantages over conventional Pulse Width Modulation (PWM) and P-I controller is used to obtain synchronization. The results are obtained on Shunt Active Power Filter simulation model.*

Key Words: Phase Locked Loop (PLL), Voltage Source Converters (VSC), Shunt Active Power Filter (SAPF), P-I controller, Space Vector Modulation (SVM).

1. INTRODUCTION

The transmission system mainly consists of the power source and the load. Nowadays the majority of loads are based on the semiconductor or microprocessors. These devices require the external vibrating frequency which is provided by the crystal oscillators and cycloconverters. Hence while operating on the external frequency these semiconductor and microprocessor devices results into the formation of harmonics which are fed back again into the system, making the grid voltage and current more noisy. Also in the electric networks, continues switching is also a major concept for the creation of harmonics. Due to these harmonics the load which is connected across the grid have to face some serious issues. One of which is heating problem. Due to the harmonics the electrical or electronics equipment fails to meet the parameters and hence overheats sometimes. Also the meters which we use to measure different parameters fail to give accurate reading because of the harmonics. It is due to the sensitivity malfunction cause by the harmonics.

Harmonics are produced by rectified loads, soft starters, switch mode power supplies (SMPS) and also devices based on controlled rectifiers and micro-processors and controllers. Some researchers have proposed a hybrid active power filter for damping the harmonics [1]. The hybrid filter consists of a small rated active filter and a 5th-tuned passive filter. The active filter is characterized by detecting the 5th-harmonic current flowing into the passive filter. It is controlled in such a way as to behave as a negative or positive resistor by adjusting a feedback gain from a negative to positive value, and vice versa.As such control schemes are unable to remove certain non linearity hence the result obtained at the final stage is lagging behind the expectations. The behavior of control scheme is responsible for the lack of result as no wind-up or removal of non-linearity is taken into account. Removal of non-linearity makes the system more stable and advantageous. Due to the non-linear as well as linear control schemes the system is not lagging in results. Non-linear expressions for the feedback are used as well as the feedback linearization is made to remove certain errors.[2],[3]. A robust nonlinear coordinated excitation and SVC controller is PI opposed to enhance the transient stability of power systems. The SVC is located at the midpoint of the transmission line in a power system. A nonlinear feedback law for the generator is found which linearize and decouples the power system model. Robust nonlinear control theory is employed to design the coordinated controller which consists of three controllers, an excitation controller and two SVC controllers. The proposed coordinated controller is designed based on local measurements. The design of the resulting controllers is independent of the operating point. Simulation results show that the proposed controller can ensure transient stability of the power system under a large sudden fault, which may occur at the generator bus terminal [4],[5].

2. MODELLING OF SAPF

2.1 Current & Voltage Sensors

In the shunt active power filter, the load is connected across the grid. The load which is having harmonics feed

the harmonics back into the system. Hence the calculations of the parameters like current and voltage for the source and load is necessary. In the shunt active power filter the compensation current is calculated by means of the source and load currents. The current and voltage sensors are the first component attached to the grid. Using this source and load currents are calculated. Further, this calculation is used to calculate the compensating current. A voltage sensor can in fact determine, monitor and can measure the supply of voltage. It can measure AC level or / and DC voltage level. The input to the voltage sensor is the voltage itself and the output can be analog voltage signals, switches, audible signals, analog current level, frequency or even frequency modulated outputs. That is, some voltage sensors can provide sine or pulse trains as output and others can produce Amplitude Modulation, Pulse Width Modulation or Frequency Modulation outputs. In voltage sensors, the measurement is based on the voltage divider.

Table -1: List of symbols

L_s, L_f	Line inductance, filter inductance
I_{dc}, V_{dc}	dc current, dc voltage
$I_{load}, I_{harmonic}$	Load current, harmonics current
I_{sa}, I_{sb}, I_{sc}	Three-phase currents
I_d, I_q	Component currents in $dq - frame$
K_p, K_i	Proportional constant, Integral constant
u_c, u	Controller output, Actuator output

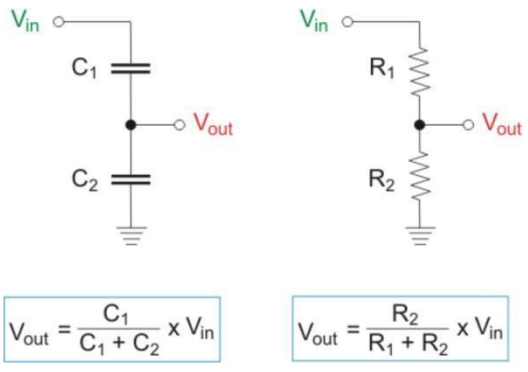

Fig -1: Principle of voltage sensors.

2.2 Synchronous Reference Frame Theory

In this paper Park's transformation is used. The a-b-c phase sequence is converted into the d-q-0 reference frame. The Idea behind the conversion of reference frame is that, the d-q-0 frame is more controllable and hence can be manipulated as per the requirement of the operation. The principle of this theory is about the transformation of current variables in synchronously rotating d-q frame. To generate the unit vectors, voltage signals are processed by the PLL. As per SRF theory, current signals (a-b-c variables) are transformed into d-q frame and then filtered. Then compensating current variables are transformed from dq frame back to a-b-c frame and fed to current controller which is used for generating switching Solar panel pulses for inverter switches. In this method, first the source current variables (Ia, Ib, Ic) are carefully detected and then transformed into two-phase stationary frame (α-β-0) from the three-phase stationary frame (a-b-c). This transformation equation is given in equation below. The a-b-c to d-q-0 frame is applied into the system after current and voltage sensing. The reason behind applying the transformation is to control the stationary reference frame. Further, applying the PI controller the lost power is calculated and fed back into the system.

$$\begin{bmatrix} Id \\ Iq \\ Io \end{bmatrix} = \frac{2}{3} * \begin{bmatrix} 0 & -\frac{1}{2} & -\frac{1}{2} \\ \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} \quad (1)$$

The a-b-c to alpha-beta conversion is applied for the shunt active power filter when the PWM is required. In pulse width modulation the stationary reference frame is converted into alpha beta sequence. The conversion is as follows:

$$f_{abc} = V_m \begin{bmatrix} \cos \omega t \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \quad (2)$$

The signal f_{abc} in the a-b-c stationary frame is rotating with the frequency ω in radian per second. The signals in α-β-0 are obtained using below equation (3)

$$f_{\alpha\beta 0} = V_m \begin{bmatrix} \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{2}{3} & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos \omega t \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \quad (3)$$

In this method the a-b-c are fixed on the same plane and are separated from each other by 120 degree phase shift. The frame in equation no (3) is still rotating and to convert

the frame into stable stationary the transformation of α-β-0 to d-q-0 is taken. This transformation in performed using equation (4)

$$B = \begin{matrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{matrix} \quad (4)$$

$$f_{dq\,0} = \begin{matrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{matrix} f_{\alpha\beta\,0} \quad (5)$$

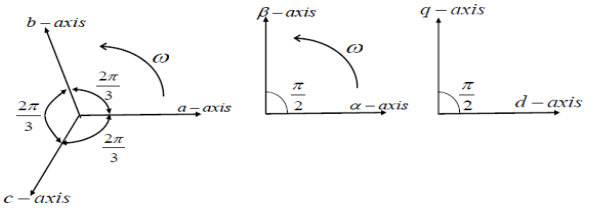

Fig -2: Reference frame transformation.

2.3 PI Controller

The P-I controller mainly consists of the proportional and the integral term. It works on the principle of comparison in which the difference (error) between the process variable (PV) and the set-point (SP), the difference between harmonics current reference signal i_h and the filter is mainly taken into account. In the thesis, the P-I controller is implemented as it has more robust control than conventional controllers. The main terms of P-I controllers is the PV and SP. By manipulating these two values one can get desired output by ease. The proportional Integral is expressed as in equation (6)

$$u_t = k_p\, e + k \int_{t0}^{t} e T \; dT \quad (6)$$

With the controller transfer function,

$$D_c\, s = k_p + \frac{ki}{s} \quad (7)$$

Where k_p, k_i are the proportional and the integral gains.

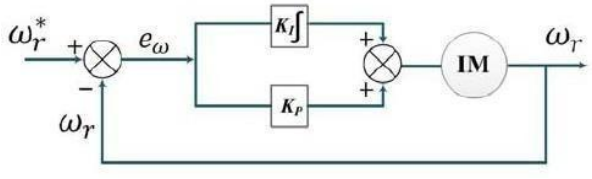

Fig -2: PI Controller

When we apply some input to the P-I controller, it compares the error between actual and set points, but some time the integrator term of the controller integrates that error causing the small unbalance in the input resulting into the large error in output of the system. Hence it is important to eliminate that phenomenon for better performance of the controller. This wind-up error is eliminated in this schematic by using the anti windup technique. Actually there are number of ways to eliminate the wind-up. But the methods in the thesis effectively compensate the wind-up.

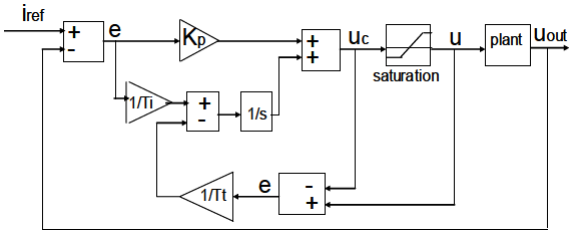

Fig -3: PI Controller with anti-windup scheme.

In this system an extra feedback path is provided by using the output of the actuator model and forming an error e_s as the difference between the estimated actuator output u and the controller output c_u and feeding this error back to the integrator through the gain $\frac{1}{T_t}$ as shown in Fig.3. The error signal e_s is zero when the signal is not saturated. When the actuator is saturated the extra feedback tries to make the error signal e_s equal to zero. This means that the integrator resets so that the controller output is at the saturation limit. The integrator is thus reset to an appropriate value with the time constant T_t, which is called the tracking time constant.

2.4 Phase Locked Loop (PLL)

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. There are several different types; the simplest is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched. The PLL is used for the applications like clock recovery, clock generation, clock distribution, frequency synthesis and noise reduction. The components of PLL are phase detector, filter, oscillator, oscillator and feedback path. The phase and frequency are interrelated by the equation (8) & (9)

$$\omega(t) = \frac{d\emptyset}{dt} \quad (8)$$

$$\emptyset\, t = \emptyset(0) + \int_{0}^{t} \omega(t)\, dt \quad (9)$$

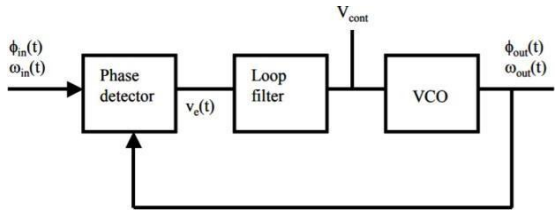

Fig -4: General form of PLL

2.5 Pulse Width Modulation (PWM)

Pulse-width modulation (PWM) is the basis for control in power electronics. The theoretically zero rise and fall time of an ideal PWM waveform represents a preferred way of driving modern semiconductor power devices. With the exception of some resonant converters, the vast majority of power electronic circuits are controlled by PWM signals of various forms. The rapid rising and falling edges ensure that the semiconductor power devices are turned on or turned off as fast as practically possible to minimize the switching transition time and the associated switching losses. Although other considerations, such as parasitic ringing and electromagnetic interference (EMI) emission, may impose an upper limit on the turn-on and turn-off speed in practical situations, the resulting finite rise and fall time can be ignored in the analysis of PWM signals and processes in most cases. Hence only ideal PWM signals with zero rise and fall time will be considered in this topic. Pulse-width modulation can take different forms. A constant-frequency (CF) PWM signal can be produced simply by comparing a reference signal, r(t), with a carrier signal, c(t).

$$Bpwm(t) = sgn\ r(t) - c(t) \qquad (10)$$

where 'sgn' is the sign function. Three types of carrier signals are commonly used in constant-frequency PWM.

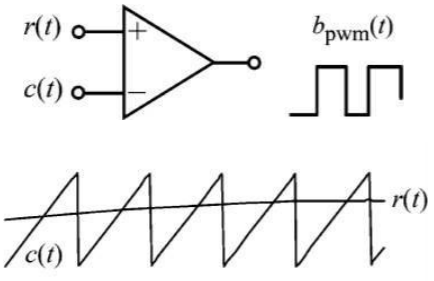

Fig -5: Reference signal & career signal

Trailing-edge modulation is most common in DC–DC converters. As will be discussed in the next section, double-edge modulation eliminates certain harmonics when the reference is a sine wave, and is a preferred method for AC–DC and DC– AC converters where the PWM reference contains a sinusoidal component. A combination of synchronized leading-edge and trailing-edge modulation has also been used to control a boost single-phase power factor correction (PFC) converter and a buck DC–DC converter to reduce ripple in the intermediate DC bus capacitor. The illustrations in Fig.6 assumed analog implementation. When digital implementation is used, the reference is usually sampled at a regular frequency and the carrier can be replaced by a counter/timer. To avoid multiple switching transitions within a carrier cycle, the reference should be sampled at the point where the carrier reaches its peak or valley. Pulse-width modulation using such sampled references is called regular-sampling PWM. To distinguish from such sampled PWM, the analog version discussed before is also called natural-sampling PWM in the literature. With a sawtooth or inverted sawtooth carrier, samples are usually taken at the beginning of a carrier cycle. With a triangle carrier, on the other hand, the reference can be sampled either once at the peak of the triangle or twice at both the peak and the valley of the triangle; the former is referred to as symmetrical sampling, while the latter is called asymmetrical sampling due to the fact that the rising and falling edge of the triangle are compared with different samples of the reference. Regular-sampling PWM is usually used in high power inverters and rectifiers and will not be further discussed in this chapter. On the other hand, the effects of sampling can be incorporated into the PWM spectral models by modifying the double Fourier integral to be presented in the following sections.

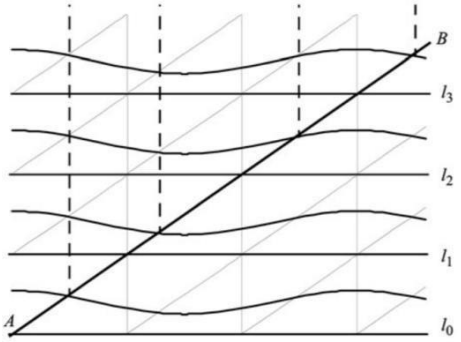

Fig -6: Reference signal & careersignal

2.5 Space Vector Modulation (SVM)

Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM). It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent

to these algorithms. A three-phase inverter as shown to the right converts a DC supply, via a series of switches, to three output legs which could be connected to a three-phase motor. The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg. i.e. if A^+ is on then A^- is off and vice versa. This leads to eight possible switching vectors for the inverter, V_0 through V_7 with six active switching vectors and two zero vectors. To implement space vector modulation, a reference signal V_{ref} is sampled with a frequency f_s ($T_s = 1/f_s$). The reference signal may be generated from three separate phase references using the α-β transform.

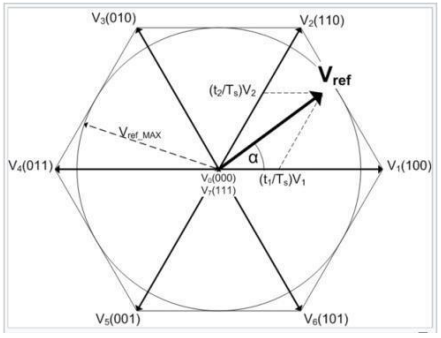

Fig -7: Switching vector for 3-leg inverter

Table -2: vector modulation table

Vector	A+	B+	C+	A-	B-	C-	Vab	Vbc	Vac	
V0 = (0,0,0)	OFF	OFF	OFF	ON	ON	ON	0	0	0	Zero Vector
V1 = (1,0,0)	ON	OFF	OFF	OFF	ON	ON	+Vdc	0	-Vdc	Active Vector
V2 = (1,1,0)	ON	ON	OFF	OFF	OFF	ON	0	+Vdc	-Vdc	Active Vector
V3 = (0,1,0)	OFF	ON	OFF	ON	OFF	ON	-Vdc	+Vdc	0	Active Vector
V4 = (0,1,1)	OFF	ON	ON	ON	OFF	OFF	-Vdc	0	+Vdc	Active Vector
V5 = (0,0,1)	OFF	OFF	ON	ON	ON	OFF	0	-Vdc	+Vdc	Active Vector
V6 = (1,0,1)	ON	OFF	ON	OFF	ON	OFF	+Vdc	-Vdc	0	Active Vector
V7 = (1,1,1)	ON	ON	ON	OFF	OFF	OFF	0	0	0	Zero Vector

SVPWM is considered a better technique of PWM implementation, as it provides the advantages such as better fundamental output voltage, improved harmonics performance and reduced THD, direct hardware implementation and very short time reaction. combination and is represented according to the phase leg connection, where 'p' denotes that phase leg is connected to the positive rail of the DC link, and 'n' denotes that phase leg is connected to the negative rail of the DC link.

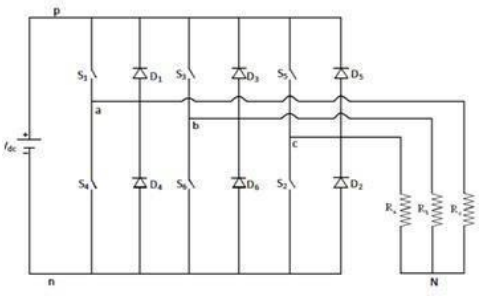

Fig -8: 3-phase voltage source inverter

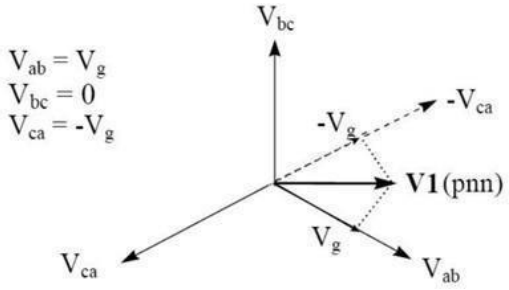

Fig -9: Topology in α-β transforms.

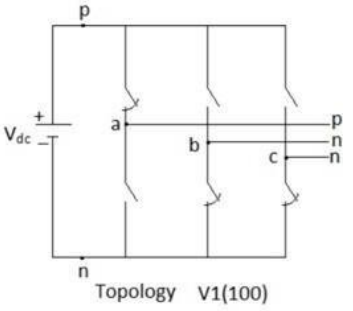

Fig -9: Topology of three phase converter

The algorithm can be expressed from the basis waveform by applying Fourier series analysis, the amplitude of any odd n'th harmonic can be expressed as

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{n} [E_k \cos n\theta_k] \quad (11)$$

Where 'n' is the odd harmonics. The amplitude of all even harmonics is zero. The modulation index 'm' is given by equation (12). The voltage Total Harmonics Distortion (THD) is given by equation (13).

$$m = \frac{\pi}{4} \frac{V_1}{\sum_{i=1}^{n} E_i} \quad (12)$$

$$THD = \sum_{n=3,5,7,\ldots}^{\infty} \frac{\overrightarrow{V_n^2}}{V_1^2} \quad (13)$$

Now to find the problem and to implement an algorithm for the following variable input of the inverter V1, V2, V3, and so on, modulation index term 'm', Output of the algorithm Θ1, Θ2, Θ3, and so on such that the THD is minimum. The input voltages are from dc source. From modulation index 'm', determine the value p of by evaluating

$$m = \sum_{k=1}^{n} e_k \sqrt{1 - (\mu_k \rho)^2} \quad (14)$$

Where,

$$e_k = \frac{E_k}{\sum_{i=1}^{n} E_i} \quad (15)$$

$$\mu_k = \frac{\sum_{i=1}^{nk} E_i - \frac{E_k}{2}}{\sum_{i=1}^{n} E_i - \frac{E_n}{2}} \quad (16)$$

$$\theta_k = \sin(\mu_k \rho) \quad (17)$$

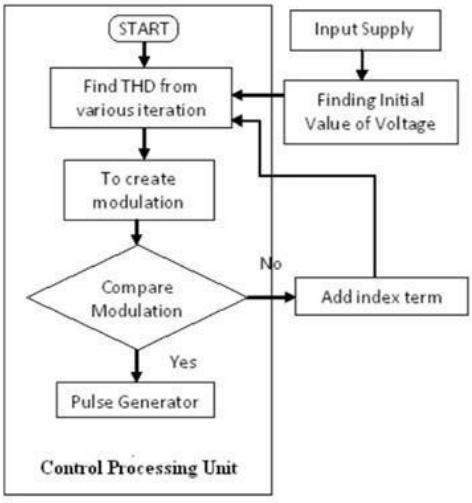

Fig -10: SVM algorithm

2.6 Estimation of reference source current

The estimation of reference source current is formulated as:

$$i_s(t) = i_L(t) + i_F(t) \quad (18)$$

Where, $i_s(t)$ - Source current

$i_L(t)$ - Load current

$i_c(t)$ - Compensating current

The utility voltage is given by:

$$V_s(t) = V_m \sin(\omega t) \quad (19)$$

Where, $V_s(t)$ - Instantaneous value of source voltage

If non linear load is connected then it has fundamental load current which is represented by

$$i_L(t) = \sum_{n=1}^{\infty} i_n \sin(n\omega t + \emptyset_n) \quad (20)$$

If active power filter provides the total reactive and harmonic power then $i_s(t)$ will be in phase with the utility and pure sinusoidal. At this time, the active filter must provide the following compensation current:

$$i_c(t) = i_L(t) - i_s(t) \quad (21)$$

2.6 Design of DC link capacitor

In this scheme the role of the DC link capacitor is to absorb/supply real power demand of the load during transient. Hence the design of the DC link capacitor is based on the principle of instantaneous power flow, equalizing the instantaneous power flow on the DC and AC side of the inverter considering only fundamental component.

$$V_{dc} i_{dc} = V_{ca}(t)\, i_{ca}(t) + V_{cb}(t)\, i_{cb}(t) + V_{cc}(t)\, i_{cc}(t) \quad (22)$$

Assuming that three phase quantities are displaced by 120^0 with respect to each other, ϕ is the phase angle by which the phase current lags the inverter phase voltage, and $2\overline{V}c$ and $2\overline{I}c$ are the amplitudes of the phase voltage and current.

Peak to peak ripple voltage is given by

$$V_{pp} = \pi * i_{pp} * X_c \quad (23)$$

In steady state the real power supplied by the source should be equal to the real power demand of the load plus some small power to compensate the losses in the active filter.

3. RESULTS & CONCLUSIONS

The input values for the active power filter are

Va = 310 V, where ø = 0°
Vb = 310 V, where ø= 120°
Vc = 310 V, where ø= 240°

For the PI controller, P = 0.1 & I = 10
Dc bus voltage Vdc = 600 V

On the basis of above results which is calculated on MATLAB Simulink, we can conclude that the THD after compensation is 1.31 percent which means there is total 10.82 percent reduction in harmonic distortion, which are under IEEE 519 standard. Fig.15. shows the voltage regulation of DC link. The voltage through the capacitor is equal to the voltage provided by the external dc link. Hence the DC link is charging through rectifier and discharging while inserting the required harmonics into the system through inverter simultaneously. Capacitor is maintaining the amount of voltage provided by DC link hence there is good voltage regulation and the link is working properly.

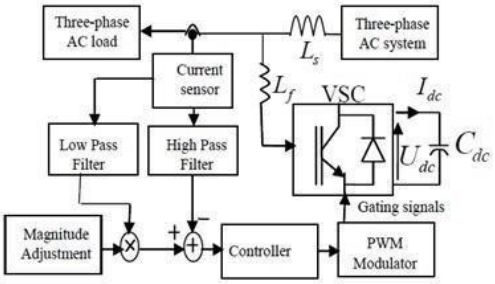

Fig -13: Schematic of SAPF

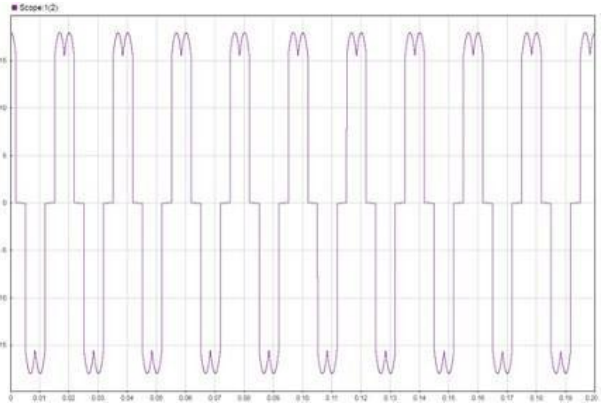

Fig -11: Load current

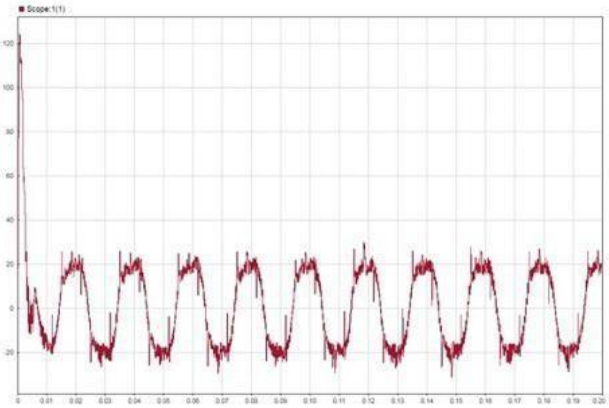

Fig -12: Source current

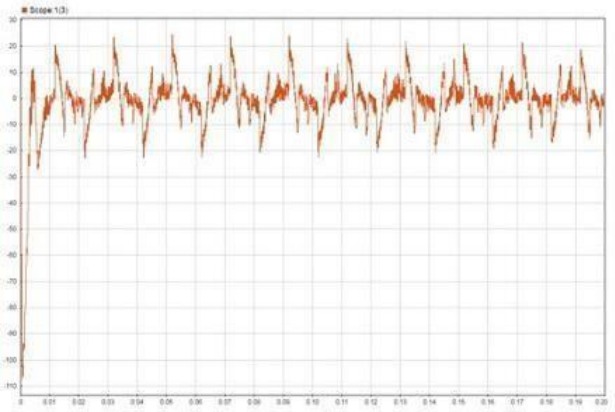

Fig -13: Compensating current

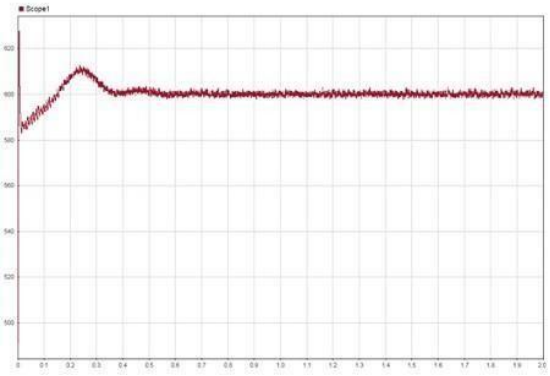

Fig -14: DC link voltage

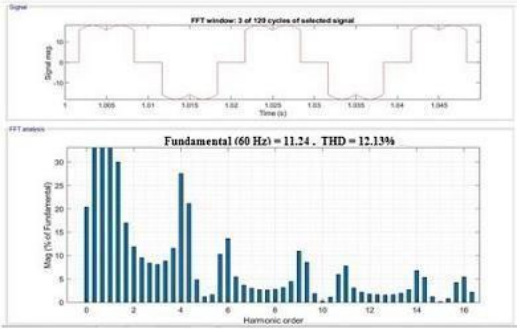

Fig -15: THD for load before compensation

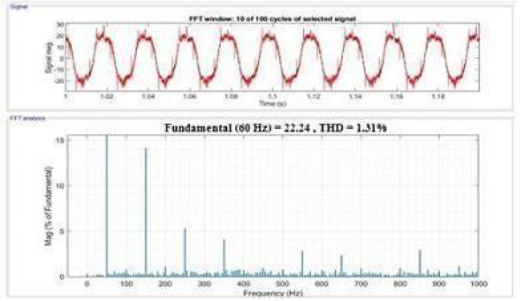

Fig -15: THD for after compensation

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