DESIGN OF pHEMT BASED LOW NOISE AMPLIFIER FOR L AND S BANDS

Mrunal A. Marihal[1], Debasish Dash[2], Dr. K. Sreelakshmi[3]

[1]Mtech-Radio Frequency and Microwave Engineering, Department of Electronics and Telecommunication Engineering, R.V. College of Engineering, Bangalore, India
[2]Mtech-Radio Frequency and Microwave Engineering, Department of Electronics and Telecommunication Engineering, R.V. College of Engineering, Bangalore, India
[3]Professor and Head of Department, Department of Electronics and Telecommunication Engineering, R.V. College of Engineering, Bangalore, India

---***---

Abstract - *The paper presents a two stage LNA for the wireless applications which comes under a larger bandwidth of 1GHz to 4GHz. The LNA uses ATF-55143 pHEMT low noise MOSFET transistor with a supply voltage of 2.7V. The LNA design has multi-stage topology, which includes 3 transistors. First stage is a CS topology while current reused topology is used to design second stage. Entire simulation is conducted by using Advanced Design System (ADS) tool. The result shows the good Gain of 24.519dB and Noise Figure of 0.68dB at the operating frequency of 2GHz. The Return Loss S11 and S22 are -14 dB and -11 dB respectively.*

Keywords: Advanced Design System (ADS), Gain, LNA, Noise Figure, pHEMT, Return Loss

1. INTRODUCTION

Nowadays in the wireless communication, new technology aims for the smaller footprint chip. The top popular source of wireless communication is mobile phone, whose wireless standards such as GPS, GSM (3G), LTE (4G), DCS, DECT, PCS-1900, WCDMA, Wireless LAN, WIFI and Bluetooth falls under a wide bandwidth of 1GHz to 4 GHz (L and S bands) [1].

Low noise amplifier is the forepart of each receiver, which is known as an electronic intensifier, used to enhance the undesirable signals [2]. In the overall performance of RF receiver, the LNA plays a critical role and its design is mainly depended on the parameters such as stability, gain, NF, operating frequency range, input-output return loss and linearity. While designing a LNA designer should take care of these parameters.

A number of different transceiver architectures have been proposed for the applications such as radio/mobile/satellite communication, military telemetry and weather/surface ship radar. Pseudomorphic high electron mobility transistors (pHEMT) are the best choice for these applications as they can provide low NF and a maximum gain. The pHEMT also demonstrate low ON resistance and a large OFF resistance. A shunt resistive feedback CMOS LNA has been designed in [3]. For polarization adjustable satellite receiver a low cost dual band LNA is presented in [4]. For wireless devices and wireless communication systems a frontend LNA is designed in [5]. In all these architectures, the first block of receiver is LNA. Designing LNA with wide band characteristics, minimum noise and high gain is challenging. Compared to single stage LNA, the gain produced by two-stage LNA is more.

To characterize the performance of the LNA different configurations/topologies are used in [6]. The LNA is designed for Zigbee standard at the working frequency of 2.4 GHz. Results shows that the lowest noise figure is produced by CS inductively degenerated low noise amplifier with FDC. A CS-cascode LNA with FDC produces highest linearity and from common source inductive degenerated LNA, highest gain is obtained. A cascade-CR structure is used to achieve a low power consumption and high power gain with intermediate inductors. It also provides a sufficient noise performance level with a better good input-output matching and an acceptable linearity.

The proposed wideband LNA design has 2 stages with LC - input and output matching networks. The CS topology with inductively degenerated source has been implemented in the first stage to have low noise figure and maintain the forward and reverse return losses below -10 dB. The current reuse technique utilizes a two stage cascade to share the same current source. CR-topology used at second stage to obtain gain more than 22dB.

Remaining structure of the paper is as follows. In section II, the LNA parameters are discussed. The design methodology of LNA is presented in Section III. Section IV discuss about the simulation results. Section V addresses the conclusion.

2. LNA PARAMETERS

There are some important parameters which checks the functionality of an LNA.

2.1 Noise Figure

Before One of the most important performance parameter of a LNA is the noise factor (F) or noise figure (NF). The NF of a receiver system, according to Friis formula is given by equation:

$$NF_{rx} = NF_1 + \frac{NF_2 - 1}{G_1} + \dots \frac{NF_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (1)$$

Where n=1, 2, 3, …

Equation (1) shows that the first stage of the receiver will be the most significant contributor for entire NF of the system. The NF of a system can be expressed in decibel, that is:

$$NF = 10\ log_{10}(F) \tag{2}$$

2.2 Gain

There are three different gains associated with LNA they are power gain (G_P), available gain (G_A) and transducer power gain (G_T). Mathematical expression of these gains are discussed below

$$G_P = \frac{P_L}{P_{IN}} \tag{3}$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} \tag{4}$$

$$G_T = \frac{P_L}{P_{AVS}} \tag{5}$$

Where P_L is the power delivered to the load of the system, P_{IN} is the power given as input to the transistor, P_{AVN} is the power available from the source of the system and P_{AVS} is the power available from the transistor [7].

2.3 S-Parameters

S-Parameters that is scattering matrix describes the connection between inputs and outputs of electrical circuits.

2.4 Stability

A two-port network is unconditionally stable if the real part of Zin > 0 and Zout > 0; for all passive load and source impedance at a given wide range of frequencies. The stability criteria is K > 1 and Δ <1.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}|^2|S_{21}|^2} \tag{6}$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \tag{7}$$

3. DESIGN METHODOLOGY OF LNA

Different types of transistors are available, which can be used for LNA applications. As the proposed LNA design works on a larger bandwidth of 1 GHz to 4 GHz, in order to achieve the low noise figure at the first stage and the maximum gain at the second stage, a GaAs pHEMT ATF-55143 transistor is used. It provides an excellent combination of low noise performance for a wider frequency range, high power output and high gain.

After selecting a transistor, the next step of designing is finding the Bias point. Here the transistor is biased on the basis of $I_{DS} - V_{DS}$ curves of the transistor. The specifications for biasing point are as follows: $V_{DS} = 2.7V$ and $I_{DS} = 10mA$.

LNA's first stage is designed by using CS topology. The protection has to be provided to DC biasing circuit from the high frequency effects of the termination ports so that the biasing of the active device the S-parameters should not change. In the middle of the DC biasing circuit and termination port, inductors are inserted to protect the biasing circuit from the effects of the termination ports. Means DC_Feeds are replaced with inductors (L). DC blocking capacitors are used, to protect termination ports from the DC voltage and DC current. Means DC_Block are replaced by capacitors (C). Two inductors are added at source in order to maintain return loss.

The current-reused topology (CS-CS) is designed at second stage. It is designed in order to obtain gain more than 22dB. Using CS-CS and CS-CG current-reused topologies, an experiment conducted by utilizing ADS software in [8]. According to the results both topologies produce nearly the same gain, but the CS-CS CR topology provides lowest NF and low power consumption with better linearity. As the common gate has substantial gate noise, common source is selected to reduce NF. Degenerating inductor at the source plays an important role in gain, return loss and stability. Figure1 shows the proposed LNA for the bandwidth of 1 GHz to 4 GHz.

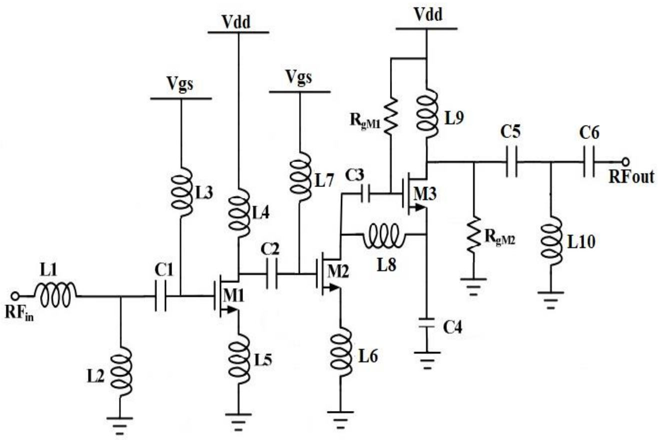

Fig -1: Two-stage proposed LNA circuit

4. RESULTS AND DISCUSSION

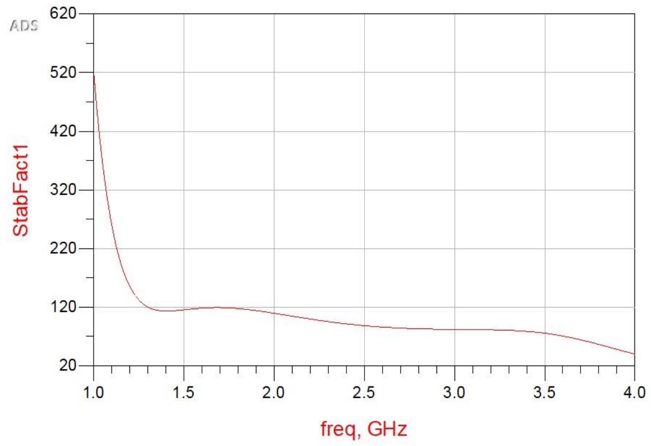

Fig -2: Stability factor of the wide-band LNA

The simulation results of LNA for the selected bandwidth are provided in this section. Stability, NF, return loss, gain are the results and their simulation plots are shown in figures 2~5. According to stability criteria the designed LNA is unconditionally stable. Here K >1; for all the frequencies as shown in Figure2.

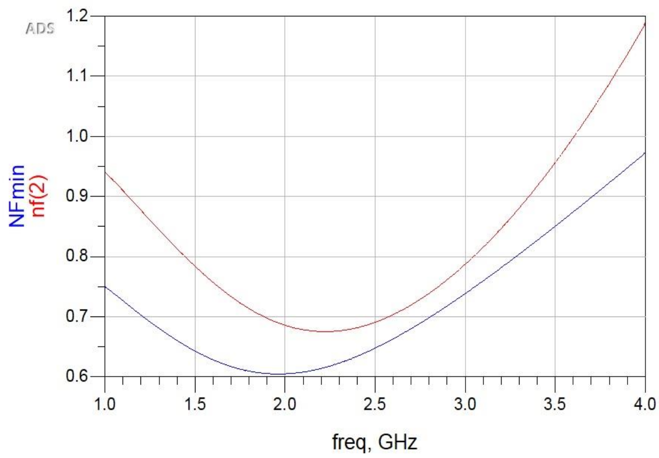

Fig -3: NF of wide-band LNA

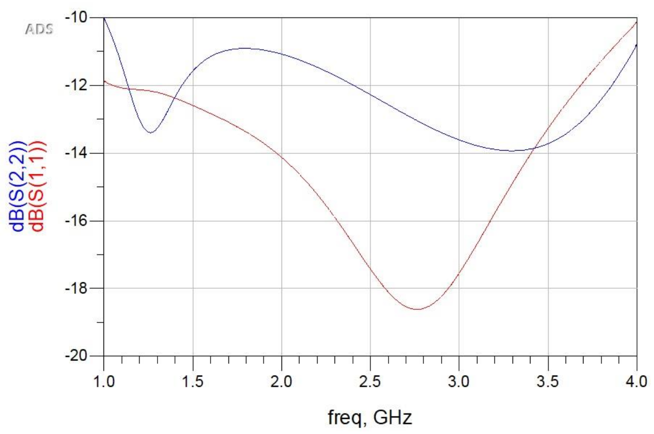

Fig -4: Return loss of wide band LNA (in dB)

A low NF is achieved through lumped matching. The minimum noise figure of 0.675dB is achieved at 2.2 GHz. As shown in figure3 the noise figure is less than 1.2dB for overall bandwidth. The simulated return loss of LNA is shown in Figure4. An input return loss of -14.129dB is achieved at 2GHz. While an output return loss of -11.080dB and -70.363dB of reverse gain is observed at the same operating frequency. The return loss S_{11} and S_{22} are below -10dB for overall bandwidth.

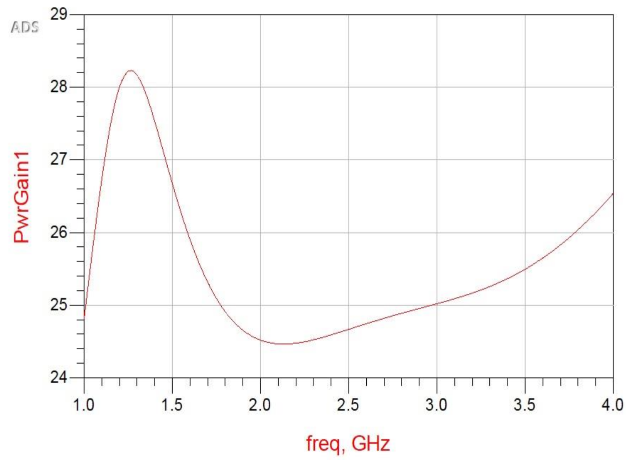

Fig -5: Gain of wide band LNA

Table -1: Comparison of proposed LNA with the state of the art

Ref.	VDD (V)	Topology	Frequency (GHz)	Noise Figure	Max Gain (dB)
[1]	4	2-Stage Cascode	0.5-3	2	22
[3]	1.2	2-Stage Cascode	2.4	1.182	15.417
[5]	4	Single CS stage	5-6	<0.68	10.6
[6]	1.2	CS Inductive Degeneration LNA with FDC	2.4	0.988	23.032
This Work	2.7	2-Stage CS-CR	1-4	0.675-1.188	24.93 to 28.23
This Work	2.7	2-Stage CS-CR	2 (Fo)	0.686	24.519

The designed LNA achieves a peak Gain of 28.23dB at 1.2GHz. At the operating frequency 24.519dB of gain is achieved. The table-1 shows the comparison of the designed LNA with other reported LNA designs. Where Fo is the operating frequency.

Table -2: Comparison of Return Loss values

Ref.	VDD (V)	Frequency (GHz)	S11 (dB)	S22 (dB)
[1]	4	0.5-3	below -6	Below -6
[3]	1.2	2.4	-9.170	-6.204
[5]	4	5-6	-12	-11
[6]	1.2	2.4	-9.408	-4.730
This Work	2.7	1-4	-11.875 to -14.979	-10.799 to -18.614
This Work	2.7	2 (Fo)	-14.129	-11.080

5. CONCLUSION

The trade-off between the NF and gain is observed in the proposed ultra-wideband low noise amplifier design. By compromising one parameter, the other one can be improved. A peak gain of 28.23dB is achieved at 1.2GHz; 0.675dB is the minimum noise figure, achieved at 2.2 GHz. The return loss S11 and S22 are observed below -10dB for overall bandwidth.

ACKNOWLEDGEMENT

It is acknowledged by the authors, that the suggestions and timely support of R V College of Engineering, Bangalore, India has greatly helped in the successful completion of the project.

REFERENCES

[1] S. Kamat, K. Sreelakshmi and R. Kumar, “Ultra wideband low noise amplifier for wireless applications,” 2017 International Conference on Intelligent Computing and Control (I2C2), Coimbatore, 2017, pp. 1-5.

[2] M. Charchian, B. Zakeri and H. Miar-Naimi, “Wideband noise figure low noise amplifier design for 3.5–4.5 GHz,” 2015 2nd International Conference on Knowledge-Based Engineering and Innovation (KBEI), Tehran, 2015, pp. 589-594.

[3] Aditi and M. Bansal, “High linearity and low noise shunt resistive feedback CMOSLNA in 2.4GHz ISM band,” 2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE), Noida, 2017, pp. 95-99.

[4] Y. Peng, F. Yang, P. Chen, H. Zhang and X. Yu, “Design of a Low Cost Dual Band Low Noise Amplifier for Polarization Adjustable Satellite Receiver,” 2018 11th UK-Europe-China Workshop on Millimeter Waves and Terahertz Technologies (UCMMT), HangZhou, China, 2018, pp. 1-3.

[5] C. K. Jha and N. Gupta, “Design of a front end low noise amplifier for wireless devices,” 2012 Students Conference on Engineering and Systems, Allahabad, Uttar Pradesh, 2012, pp. 1-4.

[6] Aditi and M. Bansal, "Design, analysis, and comparison of LNA topologies for IEEE 802.15.4 Zigbee standard," 2017 Conference on Information and Communication Technology (CICT), Gwalior, 2017, pp. 1-7.

[7] R. Ludwig and P. Bretchko, RF Circuit Design: Theory and Applications. PrenticeHall, 2000.

[8] A. Thangarajah, H. Hsu, M. Ekpanyapong, C. Punyasai, Y. Chou and N. Liu, “Design of 20-GHz low noise amplifier for automotive collision avoidance application,” 2013 International SoC Design Conference (ISOCC), Busan, 2013, pp. 119-122.