TRANSFORMER-LESS FIVE LEVEL GRID TIED INVERTER FOR PHOTO VOLTAIC APPLICATIONS

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Abstract: *A new fundamental structure of a single-phase transformer-less grid connected multilevel inverter based on a switched-capacitor structure is presented in this study. By employing the series-parallel switching conversion of the integrated switched-capacitor module in a packed unit, attractive features for the proposed inverter can be obtained such as high efficiency and boosting ability within a single stage operation. Also, using a common grounding technique provides an additional advantage of reducing the leakage current. Moreover, the presented structure generates a multilevelwaveform at the output voltage terminals which reduces the harmonics in the system. A peak current controller is utilized for triggering the gate of the power switches and controlling both the active and reactive powers. This results in a tightly controlled current with an appropriate quality that can be injected to the grid using a single source renewable energy resource.*

INTRODUCTION

In renewable energy systems like photovoltaic (PV) applications, transformer-less inverters are playing a major role in many grid connected distributed generation (DG) systems in both commercial and residential areas. The main advantages of these systems over transformer-based structures are higher efficiency, appropriate power density and lower cost. Also, removing the transformer from the output of the inverter helps in meeting some grid code requirements of many DG systems. Since the injected leakage current appears as a noisy dc offset to the grid, the major assigned regulation is controlling the value of this injected current.

The variable high frequency common mode voltage (CMV) of the inverter can generate an unwanted leakage current which can be clamped between the null of the ac grid and the parasitic capacitor of the PV array'snegative terminal. In such a condition, a resonant path is created between the output inductor base filter and the parasitic capacitor in which not only the quality of injected current is decreased but also additional power losses are produced. This phenomenon might saturate the core of other involved distributed transformers in the ac grid, the value of the leakage current for any type of transformer-less grid connected inverters. One of the simplest solutions is utilizing the Bi-polar PWM modulation strategy or half-bridge (HB) inverter instead of the full-bridge. Here, the overall variations of common mode voltage are always kept constant under any type of loading conditions; however, for

two mainreasons, the output voltage bus cannot meet other grid codes of the grid-tied systems. First, the ripple losses of the output inductor is high and second, the quality of injected power is poor. Moreover, since the amplitude of the dc supply should be compatible with the ac grid, HB-based inverters require another stage to boost the input voltage, which makes the system bulky and less efficient. Also, paralleled buck and flying inductor-based techniques, such as Karschny inverters, have utilized this concept to do so. This method has some flaws such as, having a lack of ability to support the reactive power demanded by the grid, requiring a large dc bus compatible with the peak of grid voltage, using extra deviceswhich are in line with load current and having an inability tototally suppress the leakage current under various grid conditions.

This structure can improve the performance of the system by its inherent boosting capability and unipolar PWM scheme. The fundamental components of the proposed converter include utilizing a switched-capacitor (SC) module, a virtual dc link technique and a double boosting factor capability within a single stage operation. In addition, this operation forces the input voltage to be directly connected to the output voltage terminal which causes the leakage capacitors to be shorted allowing the leakage current to be reduced to approximately zero. The structure of proposed grid tied inverter is indicated .the proposed topology consists of six power switches, two power diodes, two capacitors and an inductor.

PROPOSED SWITCHED-CAPACITOR Based GRID-TIEDINVERTER

The structure of a switched-capacitor unit as indicated in this figure, the unit consists of two power switches, one capacitor and one power diode. The switches *S1* and *S2* are both power switches with anti-parallel body diodes. Electrical operation of the SCU is based on charging and discharging of the capacitors. The charging and discharging mode of the capacitors and the current path for different modes for the SCU can boost and generate two levels of $+VDC$ and $+2VDC$ at the output voltage terminal. In other words, a virtual DC bus is generated to inject power to the Grid. This technique is illustrated. While, switches K1 and K2 are in mode (a), Capacitor C2 is charged to VDC and in mode (b), the output voltage is equal to $-VDC$. Coordinating operation of a switched-capacitor unit and virtual DC bus circuit leads to produce 0, ±VDC and ±2VDC.

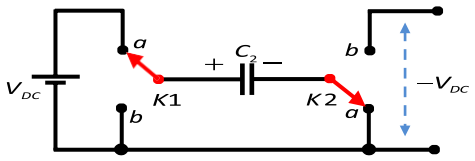

Fig. 2: Virtual DC Bus Concept.

The power switches are of unidirectional type with anti- parallel diodes.. By charging and discharging the capacitors, the proposed topology is able to boost the input source PV voltage with only a single stage.

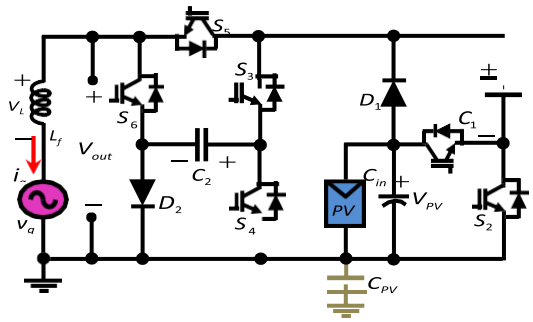

Fig. 3: Proposed grid connected inverter topology.

In addition, the negative terminal of the PV source is directly connected to the null of the grid which allows common ground capability with the proposed topology. Moreover, the inductor is acting as the output filter to smooth the output current waveform. Considering the same polarity of the grid voltage and the injected current to the grid, six different operating modes can be evaluated as depicted in the switching states for the proposed Grid-Tied inverter are addressed in Table I. In this table the charging and discharging mode of the capacitors respectively.

In the first operating mode the grid voltage is positive and C1 is in parallel with the input voltage. Therefore, the voltage of C1 increases and the inductor current rises, whereas C2 is disconnected. Hence, the output voltage will be +VPV. During the second operating mode , the grid voltage is still positive; however, to reduce the inductor current to satisfy the volt-second balance principle and to also charge the capacitor C2, switches S1, S3 and S6 are turned on in a way that the zero level can be generated at the output voltage waveform. This will lead to a decrease in inductor current in this mode. During, the third mode switches S1, S3 and S5are turned on. Again, capacitor C2 is charged in this mode and the output voltage is equal to +2VPV. Once the grid voltage becomes negative, the forth operating mode starts and the injection of the power to the grid is accomplished by the capacitor voltages on C1, C2 and by turning ON switches S2, S3 and S6. Here, by turning ON the switches S2, S3 and S6, the power diode D2 is forced to be turned off and C1 is charged to the PV voltage once again. While the capacitor C2 discharges, the inductor current linearly rises in the negative polarity. The inductor's current in the decreases to the negative polarity direction and charges the capacitor C2 to double the value of PV Voltage in the fifth operating mode. Here the switches S1, S3 and S6 are turned ON finally, the last mode occurs when the switches S2, S4 and S6 are turned on. In this mode the capacitor C2 is discharged while C1 is charged by input PV panel. Therefore, the -2VPV level is created in the -Ve half-cycle of the grid's voltage.

By using series- parallel conversion, the SC module switches in full cycle of the grid frequency, C1 can be charged in both half-cycles. Therefore, the voltage across the capacitors C1 and C2 are fixed to the value of VPV and 2VPV respectively and result in a five-level unipolar based boosted output voltage waveform. In the proposed common ground type inverter, the voltage of the PV panels can be half the value of the conventional grid-tied connection.

Modes	Switching States								C_1	C_2	V_{out}
	S_1	S_2	S_3	S_4	S_5	S_6	D_1	D_2			
Mode III	on	off	on	off	on	off	off	on	0	1	$+2V_{PV}$
Mode I	off	on	off	off	on	off	on	off	1	-	$+V_{PV}$
Mode II	on	off	on	off	off	on	off	on	0	1	0
Mode V	on	off	on	off	off	on	off	on	0	1	
Mode IV	off	on	on	off	off	on	on	off	1	0	$-V_{PV}$
Mode VI	off	on	off	on	off	on	on	off	1	0	$-2V_{PV}$

Table I. Switching States

PROPOSED CONTROL SYSTEM OF THE GRID-TIED INVERTER

In this section, the proposed modulation strategy based on the PCC technique is presented to control both the injected active and reactive powers. In this study, to generate the pulses for triggering the power switches, a peak current controller-based technique is utilized which regulates both the injected active and reactive power to the grid.

Since the PV panel is assumed as the input voltage source of the proposed inverter, a maximum power point tracker (MPPT) unit is also required for the control system. The maximum power point of the PV panel is determined by applying the conventional perturb & observation (P&O) technique to the measured voltage and current of the PVs.

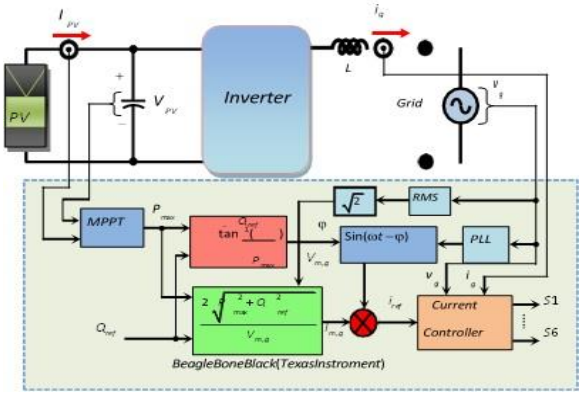

Fig. 5: Control block diagram of the proposed inverter.

Then, based on the reference value of the active and reactive powers, the required phase and amplitude of the injected current to the grid, which is known as the reference current waveform (Iref), is calculated. At this stage, the reference current waveform is sent to the current controller block for applying the PCC technique and generating the switching pulses.

The reference and measured current waveforms along with the generated switching pulses. In the current controller block, a specific sampling time (Tsam) is assigned. During the

negative half-cycle of the grid voltage, the passing current through S5 is zero. Therefore, it has no switching and conduction losses during the negative half cycle. Switches S1, S2, S3 and S6 are triggered in both half-cycles, whereas switch S5 is modulated in the positive period of the grid's frequency and switch S4 is involved in the negative half cycle. So, the corresponding switching power loss values of such switches which have no status change during one half-cycle.

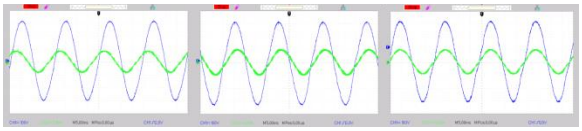

Fig. 7: logic-based diagram of switching pulses

EXPERIMENTAL RESULTS

In this section some experimental results based on laboratory prototype have been presented to validate the performance of the proposed inverter. In this case, a 24 volt PV simulator as a dc power supply has been utilized. The five-level output voltage waveform of the inverter with a peak value of 220 V which is required for injecting power to the local grid. The 50 Hz grid voltage waveform along with the five-level single-phase output voltage of the proposed inverter the positive and negative sequence of the inverter balanced, but it also eliminates any leakage current.

Element	Type	Description
S1, S2, S3, S4, S5 & S6	47N60C	650V/47A
Gate Driver	TLP 250	IC
Power Diode	MUR1560	600V/15A
Current transducer	LA55P	Hall effect
Microcontroller	Beagle Bone Black	ARM
Local grid's frequency	50Hz	-
Sampling frequency	50KHz	-
C1	6⍰20⍰F	220V
C2	680⍰F	400V
Magnetizing Inductor	Ferrite Core	2.9mH

CONCLUSION

A new topology of the single-phase grid-tied inverter has been presented in this study. The proposed topology benefits the series-parallel switching technique of capacitors and offers both boosting ability and common ground capability. Also, low total harmonic distortion is achieved through generating multilevel waveform at output voltage terminal of the proposed inverter. The capacitors employed in the SC module of the proposed inverter are balanced well by series- parallel switching conversion and handle the single stage power boosting process in the positive and negative half-cycle of the grid frequency.

Regarding the analyzed PCC technique, a tightly controlled current through a small size inductor-based filter can be injected into the grid under any demanded PF. Additionally, since the null of the grid and the negative terminal of the input source (PV panel) are commonly grounded; the problem of leakage current issues is eliminated completely. Moreover, design consideration and loss analysis of the involved switches have been developed in this study.

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