Design of 4*4 SRAM using Cadence Virtuoso in 90nm Technology

V.JEYARAMYA[1], D.GURUPANDI[2], RICHARD R[3], REKAN KUMAR S[4]

[1]Associate Professor: V.Jeyaramya, Dept. of ECE, Panimalar Institute of Technology,Chennai
[2]Assistant Professor: D.Gurupandi, Dept. of ECE, Panimalar Institute of Technology,Chennai
[3]Student, Dept. of ECE, Panimalar Institute of Technology,Chennai
[4]Student, Dept.of ECE, Panimalar Institute of Technology,Chennai

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Abstract: With the demands of upcoming technologies, further more the difficulties of nanometer-era of VLSI designs and logics require new advanced logic strategies and styles that are in the meantime elite, high performance, energy efficient and robust and immune to noise and variation. SRAM circuits are comprehensively used to plan high end circuits that result in good performance, because of their speed. Then again, the key negative mark of this circuit is high vulnerability to noise. The principle reason behind this is the sub-threshold leakage current coursing through the NMOS network of the designed system. With persistent innovation scaling, this issue is getting increasingly serious. Another noise tolerant circuit method is proposed. In the proposed work, we have upgraded the conduct of the SRAM. The proposed method provides advantage in terms of delay and power. This postulation portrays the new low power, noise tolerant method presents a correlation aftereffect of this logic with already existing method. Simulation results demonstrate that, in 180 nm CMOS technology when we utilize proposed 8T SRAM, it could accomplish minimum level of delay. Moreover, the logic also works productively with all the circuits. Atlast we infer that, the proposed scheme contributes an extremely productive is not just noise tolerant, yet in addition energy efficient and high speed.

Keywords: SRAM, DRC, LVS, RCX, Delay, Rise time, Fall time, Power dissipation.

I. INTRODUCTION

It is very challenging to design electronic gadgets with very efficient working and consume the least power. Major issues that persuade the necessity of low power design are the increase of different kind of electronic gadgets viz. smart card, audio video supported multimedia products, wireless device etc. These devices and systems need high density, high speed and low power design [1]. SRAM plays an important role in cache memory of computer, laptop, analog to digital converter, high speed registers, electronic toys, mobile phone, camera etc. The SRAM is advantageous as it does not require refreshing data until the power is ON. The maximum attainable data storage capacity of a memory chip approximate ly doubles in every two years [2]. Consistent scaling leads to the need of very high density, high performance, low leakage current, less power dissipation with low cost.

An attempt to analyze the performance of NAND and NOR gate based on CMOS technology is done. Result shows NAND gate dissipates 55.73% lesser static power, less area and less access time [3]. A 6T SRAM has been designed for low power application in 180 nm and 90 nm technologies. It is observed as scaling down occurs the dynamic power, current, rise time, fall time and area reduces [4]. It is found that leakage of a transistor is responsible for more than 40% of power dissipation occurs in the circuit. Va rious power reduction techniques like Self-Vo ltage Controller circuit, Transistor Stacking, and Supply Vo ltage Reduction, have been implemented. It has been observed that as voltage increases, the proportionate increase in leakage current occurs [5]. A 16 Kbit memory has been designed that operates at the frequency of 1.24 GHz. For cell arrays , sleep controller and power cut-off during standby mode for low leakage current are used. Programmable timing control circuit is used to mitigate the delay variation [6]. It also focused on energy analysis of SRAM with multi-threshold to reduce power dissipation and improve performance. For reducing leakage current high threshold is required for cross coupled latch and access transistor. With optimum device combination energy efficiency improved by 6.24 times whereas, optimum device combination along with performance boosting and power reduction technique shows 33 times improvement of energy efficiency [7]. Transistor sizing has the very crucial role for a read or write operation to be stable [8]. Dual threshold 7T SRAM cell is proposed and compared with the standard 6T SRAM cell. It analyses the basis of read delay, write delay, leakage power consumption and Static Noise Margin in all the three (hold, read and write) mode of operation. Single bit line is used to reduce the access time for read and write operation. The leakage power consumption and write delay are reduced by 61.50% and 66.67% respectively [9].

The detailed analysis of 6T, 7T, and 8T SRAM cell with respect to various electrical para meters is carried out. It observes the variation of dynamic power, static power dissipation and delay with supply voltage. Also an effort has been made to analyse the variation of temperature on dynamic and static power dissipation. Full custom layout design has been done successfully for the said SRAM cells and RCX completed successfully.

This paper has been organized into following steps: Section I enlists a brief introduction of previous work done. Section II has a discussion on the operation of various schematic of SRAM cells. Section III shows the Layout and its Av-Extracted view that may be used for post layout simulation. In Section IV simulated results are discussed along with tables and graphs. Section V has the conclusion of the paper.

Flowchart of Proposed work

The flowchart in Fig.1 shows the brief description of the work carried out in this paper. 6T, 7T & 8T SRAM cell schematic is designed in Cadence virtuoso. Further simulation and parameters measurement has been carried out. Layout of schematic is drawn and DRC is checked then LVS matching occurs. Thereafter, RCX test is run for Av-Extracted view for parasitic e xt raction.

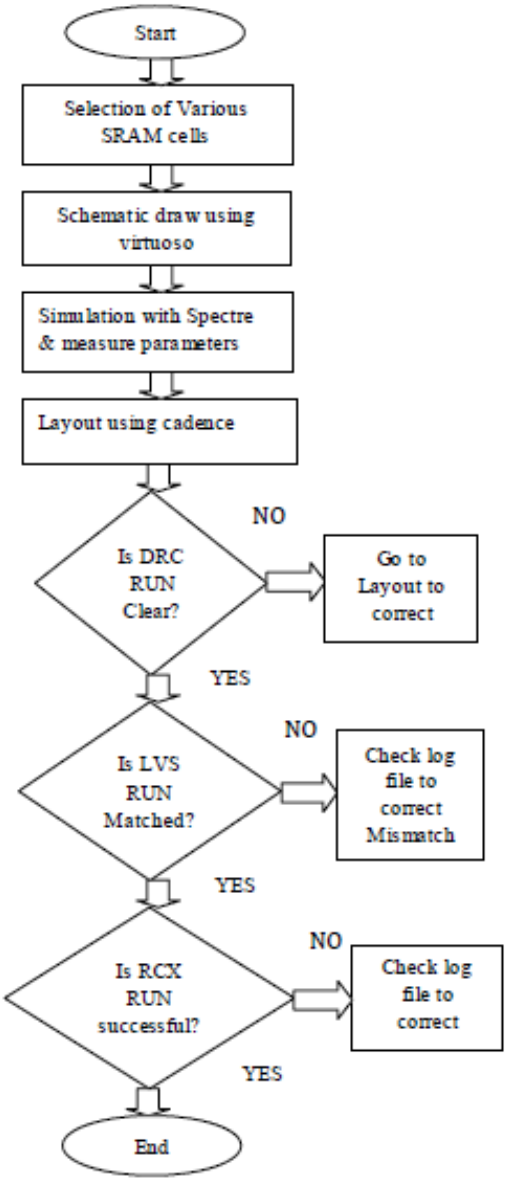
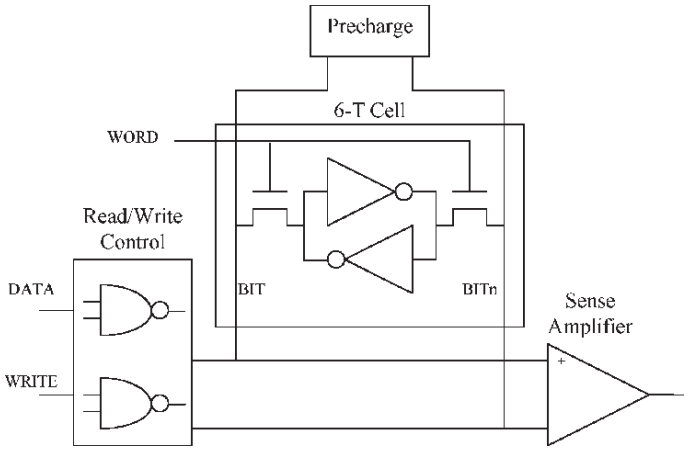


Fig. 1 Flowchart of the proposed work



II. DISCUSSION ON VARIOUS DESIGNS OF SRAM CELLS

A. Operation of 6T SRAM

A conventional 6T SRAM memory cell consists of two inverters cross-coupled to each other along with two access transistors as shown in Fig.2 [3]. The information is stored at the two internal nodes P & Q for read and write operation through access transistor.

For the read operation, first precharge bit line (BL) and bit line bar (BLB) to V_{DD} and then turn "ON" word line (WL) to activate NM3 & NM4 so that internal node P & Q make connections with BL and BLB. During write operation WL should become high and depend on the initial condition of nodes P and Q, bit "0 or 1" can be written. At hold state, WL remains OFF and BL & BLB are left floating.

Failure in read operation is sometimes observed, caused due to increase in voltage at any of nodes (P or Q) of an inverter which leads to tripping of another inverter means the voltage at another node (Q or P) starts falling resulting loss of information.

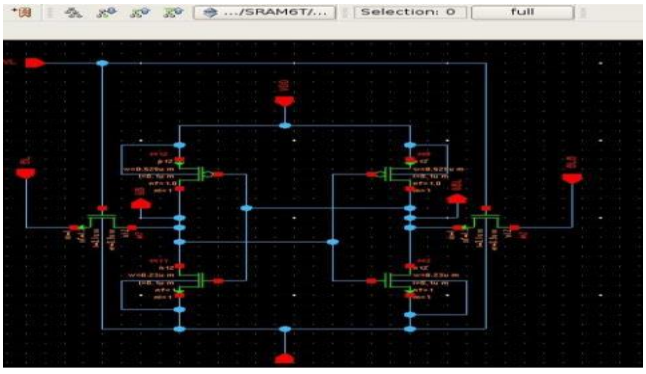


Fig.1 Schematic of 6T SRAM [3]

The output waveform shown in Fig.3 dictates the transient analysis and DC analysis of 6T SRAM cell. The analysis result shows dynamic power and static power 8.69 µW and 18.15 pW respectively.

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Fig.2 Transient and DC response of 6T SRAM

The simulations are carried at 1.8 V and the operating temperature is 27 ^{0}C.

B. 10T SRAM memory ce ll

The schematic of 10T SRAM memory cell, shown in Fig. 6 [1], consists of two inverters connected back to back, two access transistors (NM2 & NM3) and a read buffer, that consists of two transistors (NM4 & NM 5). During write operation word line WWL, bit line WBL and WBLB are used and RWL & RBL are used during read operation.

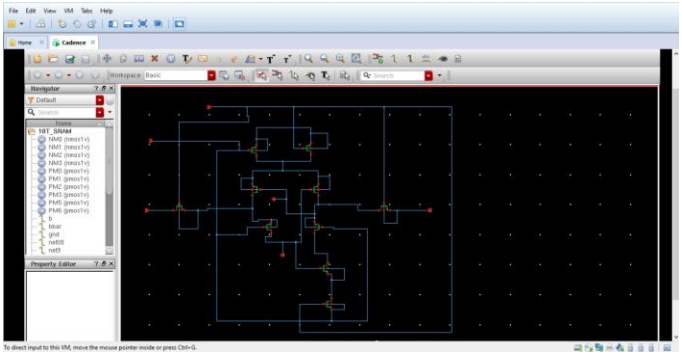

Fig.3 Schematic of 10T SRAM

The RBL precharged to V_{DD} and the current flows through the transistor of read buffer, not through the internal nodes. So the internal nodes remain at the same status as they are. The output waveform in Fig.7 depicts the transient and DC simulation for 8T SRAM cell along with dissipated power at room temperature. The result shows that it dissipates 10.55 µW dynamic power and 18.15 pW static power at the supply voltage of 1.8 V.

Fig. 4 Transient and DC response of 10T SRAM cell

Parameters	6T SRAM	10T SRAM
Delay (ns)	30.37	30.41
Frequency (MHz)	24.95	25.00
Fall time(ns)	266.3	252.1
Rise time (ns)	228.6	197.2

SRAM	Width	Length	Total Area
6T	7.72	5.20	40.18
10T	7.78	7.71	59.98

III. CONCLUS ION

A SRAM was designed using the proposed. The proposed one after simulation was compared with the simulation results of the previous proposed logic, which were simulated in same environment as the proposed logic. The outputs could be seen from the simulations. The effort has been made to find out area, delay, fall t ime, rise time, dynamic power, s tatic power, 3 dB bandwidth for different SRAM cells as shown in Table.2. The measured results show that static power dissipation is same for all the SRAM cells considered but dynamic power is least for 6T SRAM it is highest for 10T SRAM cell with 1.8 V supply voltage and 0.9 V threshold voltage. The variation of power dissipation and delay has also been observed as a function of supply voltage. The effect of temperature variation on power dissipation has also been observed. As observed from Layout, the area occupied by 6T SRAM cell is minimum and for 10T SRAM cell it is maximum..

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