AREA EFFICIENT AND LOW LATENCY BUS- BASED SYSTEM ON CHIP (SoC) ARCHITECTURE FOR INTER-PROCESSOR COMMUNICATION

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ABSTRACT: All the Digital electronic devices, like smartphones, smartwatches, video game consoles contain one or more System on Chip (SoC) that are composed by many components such as processors, memories, control units. The increasing need for data processing increased the number of processors that communicate in a SoC, Soc is a technology that integrates, different system components such as microprocessors, memory logic and DSP's into a single chip. The overall performance of SoC design depends on efficient on-chip communication architectures. Skillful interconnection architecture is necessary in inter processor communication, communication between processors and peripherals and between processor and memory. The communication architecture should be formative in such a way that it should adapt to various traffic conditions. Now a days on-chip interconnection networks are mostly implemented using shared buses which are the most common medium. The performance of SoC is improved using this probabilistic round robin algorithm with respect to the parameters, latency compared to conventional bus arbitration algorithms.

KEYWORDS: **System-on-Chip (SoC), On-Chip network, Round Robin Arbiter.**

I. INTRODUCTION

The Performance of Multicore Shared transport Embedded Controller for the most part relies upon how adequately the assets can be used. Basic transport in System on Chip is one of the sharing assets, shared by the many expert centres and furthermore going about channel between ace centre and slave centre (peripherals) or Memories. Judge is a control to use the common asset (Shared transport) adequately, so execution additionally depend on assertion methods. The mediation component is utilized to ensure that just one expert approaches the transport at any one time. The referee plays out this assignment by noticing various solicitations to utilize the transport. One of the Masters may demand to transport ace (authority) to utilize the transport during any cycle. The mediator will consider the solicitation on the ascending of the clock and afterward use predefined calculation to figure out which expert will be the close to accomplish admittance to the transport. On-chip correspondence engineering assumes a crucial part in choosing the general presentation of the System-on-Chip (SoC) plan. In the elective sharing instrument of SoC, the correspondence design should be adaptable to give elite over a wide scope of information traffic. Swifty creating gadgets industry has entered a period of multimillion door chips. It guarantees new degrees of combination on a solitary chip called framework on chip plan. Correspondence engineering plan and confirmation becomes most noteworthy need in SoC plan. The exhibition of SoC mostly relies upon effective correspondence among processor and on the steady circulation of calculation among them instead of the genuine speed of processor. Thus, there is a need for quick mediator plan and support of SoC plan.

Since, shared transport is utilized by SoC transport models, it ought to be planned in such a manner to oversee admittance to the transport, which are executed in transport mediator. Discretion is an instrument that settles the proprietor of a common asset.

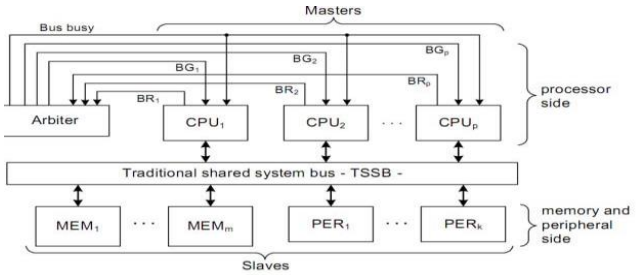


Fig.1.1 Traditional shared bus topology

Transport mediation component is utilized to protect that just one expert has the admittance to the transport at one time [3]. Transport mediator utilized plays out this capacity. Concentrated mediation is acted in this exploration. Autonomous solicitation and award signals

are utilized for each expert as utilizes need based for I/ O exchanges and fair-mindedness-based strategy among processors. To support execution, transport ought to be intended to limit the time needed for demand taking care of, discretion tending to, so that most transport cycles are used for valuable information move tasks. Transport exchange is finished according to popular demand signal continued by a reaction signal which is shown by change signal. It might restrict the most extreme number of transport cycles for expert to utilize the transport, through greatest exchange size or it might part exchanges, when slave gadgets are delayed to react to demands from an expert. Discretion conflict and transport exchange happens all the while on an equal transport with various lines. Accordingly, the correspondence engineering has a prominent job in the exhibition of SoC plan. Unified discretion is overwhelming in inserted frameworks as of late. Judge is a useful module that acknowledges transport demands from the requestor module and awards control of the common transport to each requestor in turn. Referee is a significant utilitarian module in the multiprocessor plan since it decides the correspondence between the expert and slave. It ought to be planned cautiously in elite frameworks. In this paper, likelihood based powerful transport dissemination calculation dependent on lottery strategy is. The remainder of the paper is coordinated as following: In section 2 we have investigated on different regular mediation strategies continued in the plan of SoC.In part 3 static transport assertion techniques has been shown. In section 4 we propose the portrayal of the dynamic cooperative referee. For the most part transport intervention calculation is blended and examined by transport access time or information conveyance delay. The usage of calculation is case restricted. The expanding need of on-chip correspondence has brought about different advances in correspondence engineering geography and convention plan in both industry and scholastics. As of now structures dependent on more perplexing have been proposed. Since the quantity of segments in a framework expands, intricacy of correspondence design can get outstanding prompting enormous territory and force overheads [5].

1.1 On-chip communication Topologies:

With respect to topology on-chip communication architectures can be divided as following:

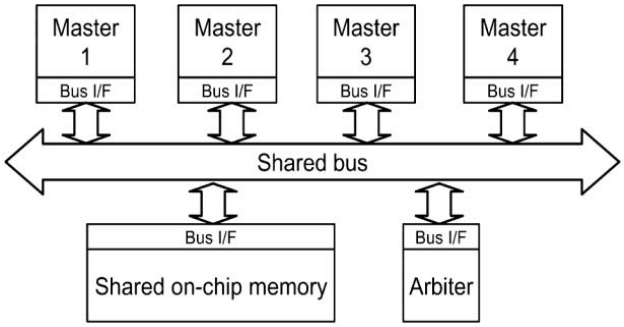


Fig. 1.2 System with Shared Bus for Contending Masters

Shared bus:

Arbitration is resolved by bus arbiter Fig.2 and the example of shared bus is system bus. Expert utilizing assertion systems referenced by the transport convention. The Bus transmission capacity is constrained by over-burdening on a worldwide transport. information bus line, longer postponement for information move, bigger energy utilization and lower transfer bandwidth.

Hierarchical Bus:

The architecture contains a few common transports interconnected by scaffolds to shape a gathering. SoC segments are put at the suitable level in the gathering as indicated by the exhibition level they request. The Low exhibition SoC segments are put on lower execution bus, which are connected to superior buss it won't trouble the better SoC parts. A few instances of such models are: AMBA transport [12], Core Connect [17], and so on. Various leveled transports offer huge throughput enhancements over the common transports in view of: I) diminished burden per transport; II) the potential for exchanges to continue in equal, on various transports; and numerous word correspondence check be gone before across the scaffold in a pipelined manner.

Ring:

In several applications, ring-based applications are widely used, such as network processors, ATM switches [18]. In a ring each node component (master or slave) communicates using a ring interface, are commonly implemented by a token pass protocol.

II. RELATED WORKS

Communication architecture design and verification becomes highest priority in SoC design and significantly affects performance, power, cost and time to market.

Hence for realizing high performance SoCs, it is important that communication architecture should be highly customized towards application traffic profiles.

2.1 Static fixed priority algorithm:

Static fixed priority is a typical planning system on most normal bus. At the point when a few experts demand at the same time, the expert with the most priority elevated will be conceded. The benefit of this assertion is its basic execute and little area cost. The static priority-based design doesn't give a way to controlling the negligible part of correspondence transmission capacity allocated to a component. On the off chance that aces with high priority demands regularly, it will prompt the starvation of the ones with low priority.

Advantages: It is simple in implement & Small area cost.

Disadvantages: In Heavy communication traffic, master that has low priority value cannot get a grant signal.

2.2 TDM/Round-Robin algorithm

Time division multiplexed (TDM) scheduling separates execution time on the bus into time slots as well locates the time slots to adapters requesting use of the bus. Each time slot can span several physical transactions on the bus. A request for use of the bus might require multiple slot times to perform all required transfers.

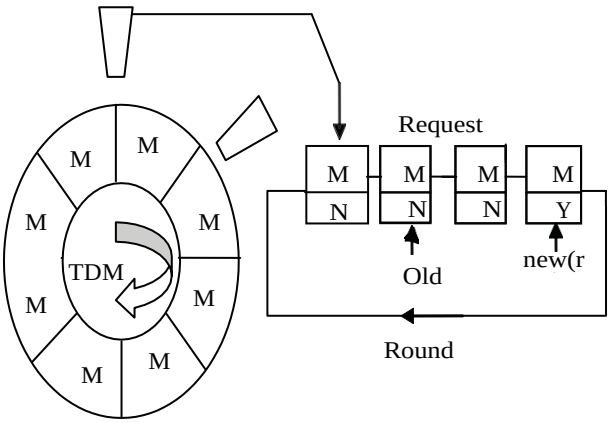


Fig. 2. 1. Round Robin based arbiter communication architecture

The first level of arbitration utilizes a planning wheel where each space is statically saved for an interesting master. In a solitary revolution of the wheel, a master that has saved more than one space is possibly allowed admittance to the channel on different occasions. In the event that the master interface related with the current space has an exceptional solicitation, a solitary word move is in all actuality, and the circumstance wheel is turned by one opening. To ease the issue of squandered openings, a second degree of mediation is upheld. The arrangement is to monitor the last expert interface to be allowed admittance through the second degree of assertion, and issue an award to the following mentioning ace in a cooperative design, at figure 3, the current space is held for M1, however it has no information to convey. The second level additions a cooperative pointer rr2 from its present situation at M2 to the following remarkable solicitation at M4.

Advantages: Easy to implement

Disadvantages: Leads to the mistake of data transfer However, these techniques are often inadequate.

The chapter presents four arbitration.

Schemes for system on chip communication as below.

• Static Lottery Bus architecture

. Dynamic lottery bus architecture

Overview of Lottery Bus Architecture:

For the Lottery bus arbitration algorithm [Fig.3.] the arbitration Is like a lottery manager, which decides which lucky one win the prize. The lottery manager accumulates the requests of bus accesses from all of the masters, an each master is statically assigned a number of "lottery tickets" [7]

A pseudo random number is generated which corresponds to one ticket Number. Based on the requests and tickets owned, partial sum is obtained, which is compared with random number.

III. EXISTING METHOD

The main of the LOTTERY BUS architecture is an arbitration algorithm implemented in a centralized "lottery manager" for each bus in the communication architecture. The architecture does not pursue any fixed topology. Hence, various SoC components may be interconnected by an arbitrary network of shared channel so flat system wide bus.

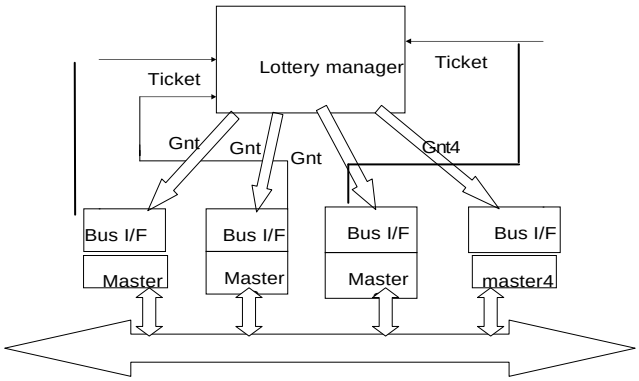


Fig. 3 shared lottery bus architecture

director pseudo-haphazardly picks one of the fighting experts to be the victor of the lottery, preferring aces that have a bigger number of tickets, and awards admittance to the picked ace for a specific number of bus cycles.

The lottery manager collects demands for responsibility for bus from at least one, every one of which is (statically) relegated various "lottery tickets," The yield is a bunch of award lines (again one for every master that show the quantity of words that the at present is permitted to move across the transport. The intervention choice depends on a lottery.

4.Dynamic lottery bus architecture

In this architecture (figure 5), the inputs are (r0r1r2r3), and the number of tickets currently possessed by each corresponding master that are generated by ticket generated by ticket generator. Therefore, under this architecture, not only Range of current tickets. Therefore, at each lottery, the lottery manager. Needs to calculate for each component Ci, the partial sum

$$\sum_{j=1}^{N} r_j * t_j$$

This is used using a bit wise AND operation and tree of adder, as shown in figure 5. The final result, T=r0t0+r1t1+r2t2+r3t3, defines the range in which the random number must lie. A limitation of this implementation is that distribution of the resulting random number is not uniform. The rest of the architecture consists of comparison and grant hardware, and follows directly from the design of the static lottery manager.

IV. PROPOSED METHOD

The bus masters beC1, C2, C3, C4 and the number of tickets held by each master are t1, t2, t3, t4.At any bus cycle, let the Boolean variables ri (i=1, 2…, n)

where ri=1 if component Ci is 1 . The probability of granting component Ci is given by

$P(C_i) = {}_n r_i * t_i$

$\sum_{N} r_j * t_{j-1}$

Then it controls the transfer of data between selected master and slave. It is noted that the grant signal is enabled after the comparison of random number and if it lies in the appropriate range, bus is shared to respective component. This architecture is simulated using ModelSim and latency is observed for various components

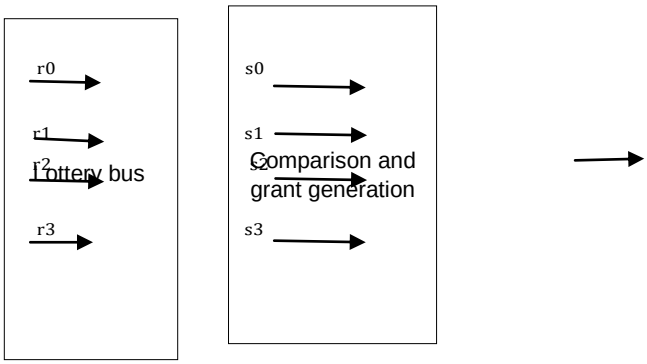


Fig. 4.1. Illustration for lottery bus-based arbiter communication architecture.

Fig. 4. 1. shows an example where three out of four bus masters have contending requests, with tickets in the ratio 1:3:4. This is given by

$$\sum_{j=1}^{N} r_j * t_j$$

In general, lies in the range

$$\left[\quad {}_{Ii+1} \quad \right]$$

$$\left| \sum r_k * t_{k'} \sum r_k * t_k \right|$$

$$\left\lfloor {}_{k=1} \quad {}_{k=1} \right\rfloor$$

it is granted to component Ci+1 The component with the largest number of tickets occupies the largest fraction of the total range, and is consequently the most likely candidate to receive the grant, provided the random numbers are uniformly distributed over the interval 1.

$$\left| 0, \sum_{j=1}^{n} r_j * t_j \right|$$

(1) Lottery manager: -In this block r1, r2, r3, r4 are the requests signal of the master and t1, t2,
t3 and t4 are the tickets of the master respectively. That will
(2) Random number generator: -
Random number generator is chipping away at the rule of pseudo arbitrary double sequence generator. (3) Comparison and award age equipment: - The random number is analyzed in equal against every one of the four halfway entireties. Each comparator yields a "1" if the random number is not exactly the incomplete aggregate at the other info. Since for a similar number, different comparators may yield a "1" it is important to pick the first, beginning with the first comparator. For instance, for the request map 1011 if the created random number is 5, jest's C4 related comparator will yield a "1." However, on the off chance that the produced arbitrary number is "1," all the

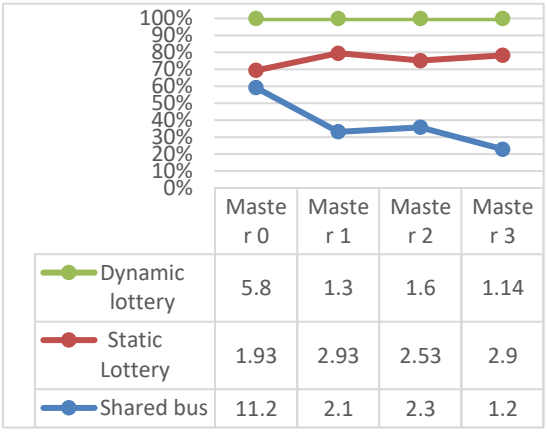
comparators will yield a "1," yet the champ is C1. The design is model utilizing VHDL for three masters. t3 are tickets esteems and gnt0, gnt1, gnt2 and gnt3 are award signs of the expert processor. Signal n1 is arbitrary number produced sign and sign h0, h1, h2 &h3 are determined an incentive for the expert or processor as indicated by its ticket worth and signal r. Figure 4 shows the recreation results for static lottery bus according to the calculation. The numbers in the recreation results demonstrate the quantity of bus getting the award of shared bus usage.

V. TESTING METHODOLOGY

The master uses the signal to the arbiter. The arbiter resolves the priority among the contending masters by comparing the generated random number with the active tickets. (he). The latency is calculated by observing the number of cycles for certain operation. Here the masters are assumed to perform read and write operation after the bus is granted.

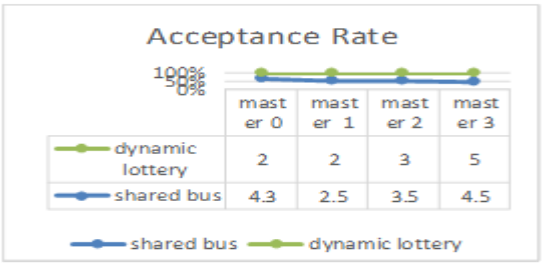
VI. PERFORMANCE ANALYSIS

The proposed architecture is demonstrated utilizing VHDL apparatus (Model Sim). It is outlined utilizing the accompanying waveforms Fig.6.In the given representation signals are appeared for the solicitation map 1011 which shows that aside from Master (C2), other three experts demand for access of the transport. Likewise, waveforms have been noticed for different maps 0111,1110 and 1101 which relates to demand signs of masters1,2,3 and 4 separately. Tickets are given by t0, t1, t2 and t3 individually. Signs ho, h1, h2 and h3 are the determined dynamic ticket esteems. The award signals are shown by g0, g1, g2 and g3 for the experts. The normal dormancy is discovered to be high for low need parts that are ace claiming least number of tickets yet discovered to be superior to static need and cooperative technique [Fig.6]. When the award signal g3 for ace M3 is noticed the postponement is discovered to be around 240 ns. For the powerful lottery bus tickets are produced progressively as they are dynamic [Fig.7.].



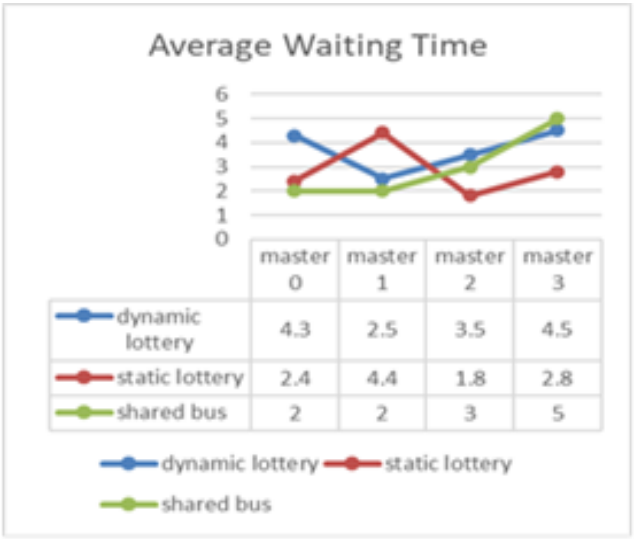
	Master 0	Master 1	Master 2	Master 3
Dynamic lottery	5.8	1.3	1.6	1.14
Static Lottery	1.93	2.93	2.53	2.9
Shared bus	11.2	2.1	2.3	1.2

Fig. 6.1 Latency



	master 0	master 1	master 2	master 3
dynamic lottery	2	2	3	5
shared bus	4.3	2.5	3.5	4.5

Fig. 6.2 Acceptance Rate



	master 0	master 1	master 2	master 3
dynamic lottery	4.3	2.5	3.5	4.5
static lottery	2.4	4.4	1.8	2.8
shared bus	2	2	3	5

Fig. 6.3 Average Waiting Time

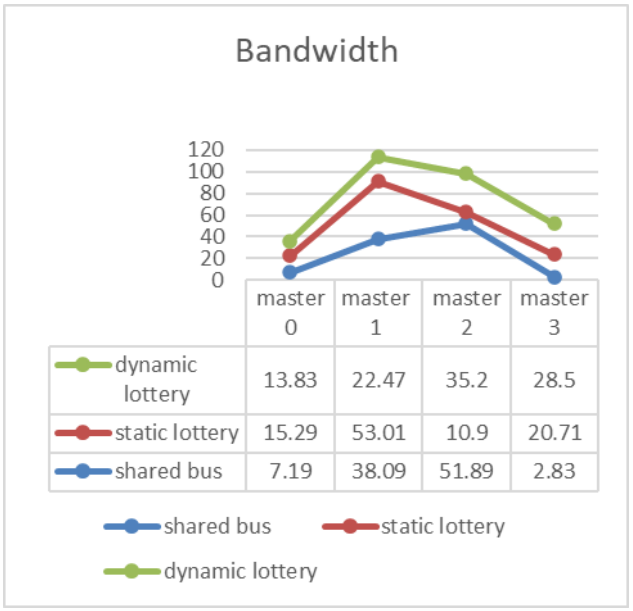


Fig. 6.4 Bandwidth

VII. EXPERIMENTAL RESULTS

At first the testing of referee incorporates giving information signs to the authority block like reqi; clock, reset and consequently noticing the yield signals like award signs to the different experts and yield esteem which is the arbitrary number. It is seen that award signal is empowered after the correlation of irregular number and in the event that it lies in the fitting reach, transport is shared to individual part. The engineering is reproduced utilizing ModelSim and idleness is noticed for different parts. Idleness for master3 is seen to be diminished around 150 ns with clock time of 10 ns in the proposed likelihood-based lottery calculation. It is discovered that under TDMA based structures, parts with higher need could encounter higher idleness than with lower need. The judge proposed in this paper doesn't show this marvel, bringing about low latencies for high requirement.

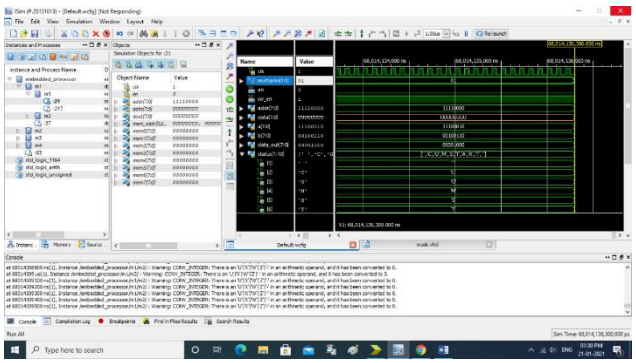


Fig. 7.1 Simulation result of dynamic lottery bus arbiter with rotating priority start.

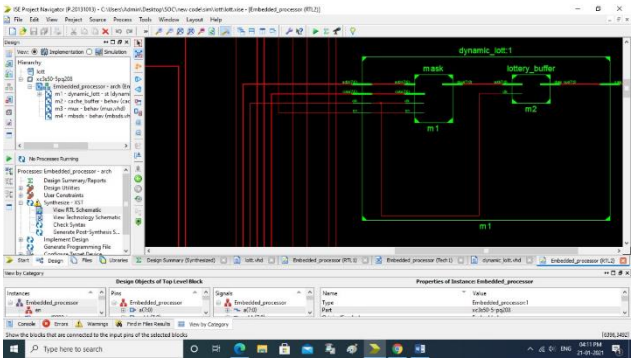


Fig. 7.2 Internal view of Dynamic Lottery Bus Architecture

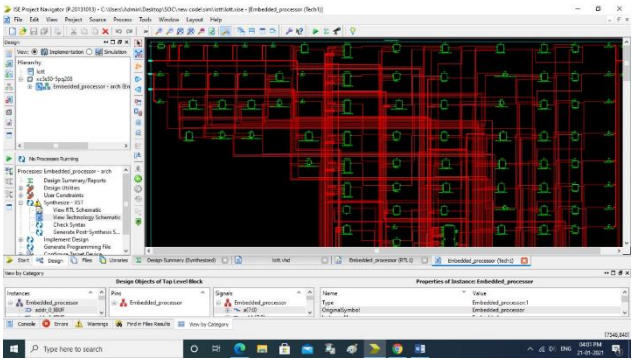


Fig. 7.3 Internal view of processor.

VIII. CONCLUSIONS AND FUTURE ENHANCEMENTS

Static priority and other conventional architectures had the drawbacks like bus starvation and bus contention when more than one master request for the bus. Hence this dynamic round robin arbiter based on lottery method is proposed. It is observed, latency is improved and attends to all masters requesting for the bus. At a time only one master will be granted the bus. This arbiter provides flexible design for efficient SoC. This algorithm can be implemented in the design of Soc which has its application in the field of communication and can demonstrate its superiority over other conventional architectures. Research is focused on employing this dynamic arbiter in AMBA based MPSOC and performance will be analyzed.

REFERENCES

[1] Ahmed Amine Jerraya, Wayne Wolf, Multiprocessor Systems-on-Chips [M], Morgan Kaufmanns Publishers Inc. San Francisco, 2005, pp.118.

[2] K. Lahiri A.Raghunathan,"The LOTTERYBUS on-chip Communication architecture", IEEE Trans. On VLSI system, June 2006.

[3] K. Lahiri, Lakshminarayan, "LOTTERY BUS:New High Performance Communication Architecture for System-on-Chip Designs",Proc.Design Automation Conference,pp.15-20,2001.

[4] Kanchan, Dinesh Padole and Dr.Preeti Bajaj, "A Design Approach to AMBA Bus Architecture With Dynamic Lottery Arbiter", Proc.INDICON, 2009 IEEE, pages 1-4.

[5] Dinesh Padole, Deepsheekha,"Fuzzy Logic Arbiter for Shared Bus Multiprocessor System : A Design Approach" First International Conference on Emerging Trends in Engineering and Technology ,2008 IEEE.