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CURRENT CONTROL OF A MULTI-LEVEL VOLTAGE SOURCE x INVERTER

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ABSTRACT-In most high-performance applications of voltage source pulse-width modulation inverters, current control is an essential part of the overall control system. This paper propose current control of a seven-level topology for medium-voltage high-power applications. This topology has fewer active switches and components, and less control complexity in comparison to the other existing classic and advanced seven-level topologies. A comprehensive review has been done on seven-level topologies to demonstrate the advantages of this topology in this project. A control method based on model predictive control (MPC) is developed to balance the flying capacitors of this topology at their desired values and control the output currents without the need of pulse width modulation blocks, and proportional-integral (PI) controllers, which is the advantage of MPC in power electronics applications. The simulation and experimental results describe and verify the current control technique for the inverter.

Keywords: PI controller, model predictive control, multilevel inverter, PWM

1 INTRODUCTION

An inverter, also named as power inverter, is an electrical power device which is used to convert direct current (DC) into alternating current (AC). Using few control circuits and switches, one can get AC at any required voltage and frequency. Inverter plays exactly the opposite role of rectifiers as rectifiers are used for converting alternating current (AC) into direct current (DC). There are different types of inverters available these days. You should also have a look at Pure Sine wave Inverter Design with code and Modified Sine Wave Inverter Design with code.

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. Mostly a two-level inverter is used in order to generate the AC voltage from DC voltage. Now the question arises what's the need of using multilevel inverter when we have two-level inverter. In order to answer this question, first we need to look at the concept of multilevel inverter.

This is an important fact which cannot be denied that the conventional sources like oil and gas began the industrial revolution. The importance of conventional sources cannot be over looked and gave tremendous growth in power sector. These conventional sources are extracted from earth crust and due to vast usage of these sources create a scarcity of resources. Burning of these conventional sources emits heavy pollution. Due to the emission of flue gases by conventional sources when burned, the processing plants with conventional fuels as main source are located far away from domestic areas [1-3]. Power plants running with conventional sources when located at remote locations impart transmission losses. There is every need to shift the process of utilizing conventional sources to alternate sources to overcome the disadvantages of using conventional energy sources. Renewable energy sources are a very good found, replacing conventional energy sources. Renewable sources are the energy sources which cannot be depleted and emits almost zero pollution [4]. Renewable energy sources are freely available from nature and the use of renewable sources can be helpful in preserving conventional sources for near future. Photo-voltaic (PV) solar energy, wind energy and fuel cell are some of the mostly incorporated types of renewable energy sources. PV system is one renewable source used for electricity generation and PV system [5-6] generates DC type of power. PV system generates low voltage and a boost converter is used to amplify the output voltage of PV system. Inverter converts the DC output of PV and boost converter to AC type to feed load. Conventional two-level inverter gives out two-level square wave output and contains high harmonics with respect to reference sinusoidal signal. Two-level inverter imposes heavy stress on power switches of the inverter. By increasing the levels in the output signal of the inverter circuit, distortion and stress can be reduced and this can be achieved by using multi-level inverters [7-10].

.Xiaonan Zhu et al [11] propose the multilevel inverters are preferred solutions for photovoltaic (PV) applications because of lower total harmonic distortion (THD), lower switching stress and lower electromagnetic interference (EMI). In order to reduce the leakage current in the single-phase low-power PV inverters, a five-level transformer-less inverter is proposed in this paper. A total of eleven switches are required, while six of them only withstand a quarter of the dc-bus voltage, so the costs for them are low. Another four switches are turned on or off at the power line cycle, the switching losses for them are ignored. In addition, the flying-capacitors (FCs) voltages are only a quarter of the dc-bus voltage, and they are balanced at the switching frequency, which further reduces the system investment. Mohammad Sharifzadeh et al [12] present a modified selective harmonic mitigation pulse amplitude modulation (SHM-PAM) is presented to be capable of canceling all triplen harmonic orders and suitable for single-phase application of five-level type of voltage source inverters. To this end, a new constraint is established for the two switching angles (α 1, α 2) to derive the new formula for the harmonics' amplitude, which results in self-elimination of all triplen harmonics (e.g., 3rd, 9th, 15th ...). The fifth and seventh harmonic orders are mitigated through normal operation of the proposed SHM-PAM technique. It is also shown that the proposed technique is extendable to other multilevel voltage waveforms and a flowchart of self-elimination of all triplen harmonics has been presented. Mathematical analysis supported by experimental investigations show the desired performance of the proposed SHM-PAM algorithm on a two-cell single-phase cascaded H-bridge inverter as a typical five-level configuration in dealing with linear and nonlinear loads. TeenuTechela Davis et al [13] present a carrier-based modulation technique is used for boosting the dc bus utilization, which is established by providing detailed mathematical analysis. The five level inverter used here is realized by cascading a CHB unit to each phase of a three-level neutral point clamped inverter. The increase in dc bus voltage utilization owes to the pole voltage redundancies offered by CHB units. The floating capacitors of H-bridge units are balanced within a quarter fundamental cycle using the switching state redundancies of pole voltage levels. The aforementioned modulation technique allows the inverter to enhance the dc bus utilization from 0.577 "dc to 0.63 "dc under unity power factor. This enhancement is obtained in the linear modulation range without increasing the dc bus voltage, and thus, the inverter can operate without the presence of low-order harmonics in its phase voltages. The strength of this paper lies in its detailed mathematical analysis for finding out the limiting modulation index and power factor condition in the light of floating capacitor voltage balancing issue.

2. EXISTING SYSTEM

The Literature survey discussed by the different authors are as follows, which all explains the existing systems. XiaoqiangGuo et al [14] propose the conventional single-phase multilevel current source inverters suffer from the high count of switches for increasing the levels. Therefore, how to generate more levels with reduced-count of switches is attractive. A programmable single-phase current source inverter is presented. It can achieve the programmable level output with only five switches. Different from the existing single-phase reduced-count multilevel inverters, it has the advantages of a simple structure and programmable level output. FelipeBovoliniGrigoletto et al [15] present an inverters are extensively employed in grid-connected photovoltaic (PV) generation systems due to its advantages of achieving low cost and high efficiency. However, the common-mode voltage issues have been motivated the proposition of new topologies, control, and modulation schemes. In common ground PV inverters, the grid neutral line is directly connected to the negative pole of the dc bus. Therefore, the parasitic capacitances are bypassed and the leakage current can be eliminated. In this paper, a five-level common ground transformer less inverter with reduced output harmonic content for PV systems is proposed. In addition, the proposed inverter can process reactive power and it presents a maximum dc-voltage utilization in opposition to half-bridge-based topologies. The operation modes of the proposed inverter, a simple modulation strategy, as well as the design guidelines are analyzed in detail. MdNoman Habib Khan et al [16] presents a novel switched capacitor (SC) based (2n + 1)-level single-phase inverter with a reduced number of components and input dc voltage supply. This inverter is designed in a way that just one dc source is required to generate different voltage levels. The circuit consists of three major parts, i.e., front-end boost stage, active SC cell(s) in the middle, and H-bridge inverter at the end. The total number of output voltage levels is up to (2n + 1) levels, where n ≥ 2 is the number of switching cells, which consists of three active switches and two capacitors. Compared with conventional SC-based multilevel inverter topologies, the proposed topology features many advantages, such as low number of semiconductor devices, quasi-resonant charging of capacitors that reduce the inrush current and current stress on the devices, self-balancing of capacitor, and reduced voltage stress on the switches. Moreover, a simple sinusoidal pulse width modulation technique is employed here to generate the modulation signals for the proposed inverter. The operating principle is presented in detail followed by comparative analysis, thermal modelling, and design guidelines.

Naima Arab et al [17] presents the current control design procedure of a single-phase grid-tied five-level packed U-cell inverter (PUC5) with an LCL output filter. The PUC5 inverter is used as an interface of renewable energy sources, such as solar applications. The LCL filter is calculated according to the grid-tied operation and converter ratings. An optimal controller, based on a linear quadratic regulator with integral action, is designed to inject a sinusoidal current with low harmonic distortion at unity power factor. For that design, the PUC5 inverter is modelled in the D-Q frame. The sensor less voltage control is incorporated into the switching technique to balance the PUC5 capacitor voltage and generate a five-level waveform at the output. Experimental tests are performed on a laboratory benchmark to confirm the theoretical design.

Ahmad H. Sabry et al [18] proposes a transformer less five-level inverter with zero leakage current and ability to reduce the harmonic output content for a grid-tied single-phase PV system. The neutral of the grid links to a common on which the negative and the positive terminals of the DC-link are connected via parasitic capacitors that can eliminate the leakage current. The proposed topology, with its inherent circuit structure, leads to boost the overall efficiency. NaserVosoughi et al [19] the proposed inverter can be obtained such as high efficiency and boosting ability within a single stage operation. Also, using a common grounding technique provides an additional advantage of reducing the leakage current. Moreover, the presented structure generates a multilevel waveform at the output voltage terminals which reduces the harmonics in the system. A peak current controller is utilized for triggering the gate of the power switches and controlling both the active and reactive powers. This results in a tightly controlled current with an appropriate quality that can be injected to the grid using a single source renewable energy resource .ApparaoDekka et al [20] propose the operation of the series-connected multilevel inverter is presented for a five-level operation, and it is realized by using two three-level half-bridge diode clamp converter modules per phase. Hence, each phase of the series-connected multilevel inverter requires a single isolated dc source. In the series-connected multilevel inverter, the net dc-bus voltage will be equally distributed between four dc-bus capacitors. Therefore, the converter generates a multilevel voltage waveform with uniform steps and ensures equal voltage stress on the semiconductor devices. To achieve these objectives, a space vector pulse width modulation scheme with an additional voltage balancing approach is employed.

3. PROPOSED SYSTEM

The need for higher power quality, operation at higher voltage levels, lower switching loss, and eliminating interface transformers in applications such as; renewable energy conversion, motor drives, reactive-power compensation, and transportation applications caused the emerge of multilevel converters in the industrial applications in recent years. The aforementioned requirements are the multilevel features, which is the advantage of these converters in comparison to conventional two-level converters. Beside the two-level voltage source converter (2L-VSC), classic and advanced multilevel topologies are proposed and studied in the literature for medium-voltage high-power applications.

Flying capacitor (FC), neutral point clamped (NPC), and cascaded H-bridge topologies are conventional multilevel topologies, which are widely used and investigated for various applications. The most used topology in the traction applications still is the 2L-VSC, however, for medium-voltage high-power applications, manufacturers commercialized different topologies such as; Three-level NPC (e.g. ABB, Siemens), Four-level FC (e.g. Altsom), CHB (e.g. Robicon, Rockwell).

Using these conventional topologies for higher voltage and power levels requires an increase in the number of levels, which is not practical since the number of components will increase substantially with respect to the number of levels. Also, challenges such as; voltage balancing of neutral points and flying capacitors in NPC and FC converters, the need of bulky transformers to provide isolated dc sources in CHB converters limits their applications in higher voltage and power applications and significantly increases the manufacturing cost of the overall converter.

However, due to modularity, convenient maintenance of the CHB topology, it is still used for the higher number of levels. For instance, seven-level CHB manufactured by Rockwell Automation. Advanced topologies have been proposed and studied to reach a higher number of voltage levels employing a few numbers of isolated-gate bipolar transistors (IGBT), diodes, and capacitors with lower voltage ratings in literature such as in, to mitigate the drawbacks of conventional topologies. Some of these advanced topologies are commercialized by manufacturers, such as five-level ANPC by ABB.

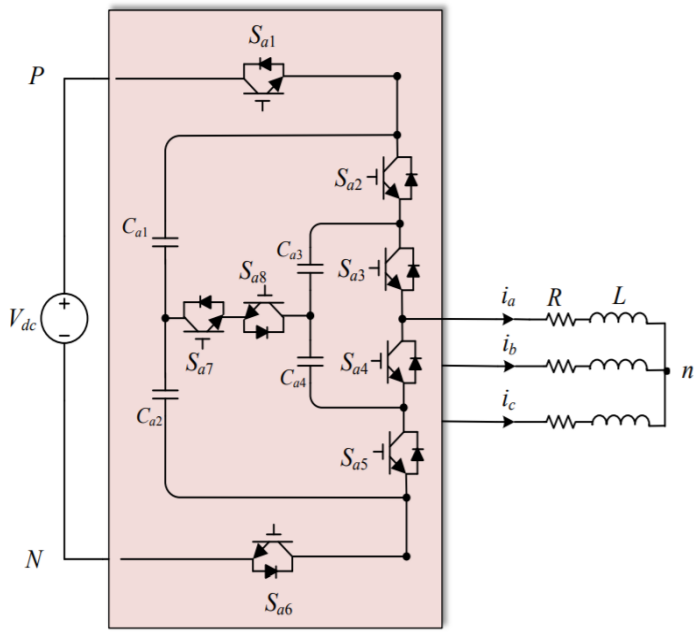


Figure 1 One-phase circuit diagram of the seven-level topology

In this project, a seven-level converter is presented, shown in Figure 1, which is an upgrade from the six-level converter proposed. This topology is a combination of flying capacitor topology and a neutral point piloted (NPP) topology. The presented seven-level converter can generate seven voltage at the output if the flying capacitor voltages are balanced at the desired values, which are Vdc/3 and Vdc/6 for outer and inner flying capacitors respectively. Vdc is the dclink voltage.

This converter consists of 8 active switches with the same voltage rating since each active switch blocking voltage is Vdc/3. This converter has a fewer number of components in comparison to other existing seven-level topologies as investigated in follow, which leads to lower manufacturing cost. A control method based on Model Predictive Control (MPC) is developed to control output currents and balance the FCs voltages at the desired values. MPC has been widely used in motor drive application recently due to its significant dynamic performance, and no need of PID controller for output current control of the converters.

Balancing the FCs voltages and tracking the output current reference simultaneously is the advantage of employing a control method based on MPC for this 7-level topology. Using a PI controller to regulate output currents requires modulation schemes such as SPWM or SVM to control the converter and balance the flying capacitors. Due to the low number of redundant switching states in this topology, controllers based on SPWM and SVM schemes are not able to regulate the FCs voltages' in all operating conditions.

In SPWM, the redundant switching states of each level, are used to balance the FCs voltages, however, in this topology redundant switching states are available only for mid-levels. In addition, in the SVM modulation scheme, the available switching states for regulating the FCs voltages are limited to the adjacent vectors, and cannot guarantee FCs voltages balancing in all operating conditions. MPC has also better performance in transient conditions and it doesn't need to tune PI parameters.

3.1 ADVANTAGES OF THE SEVEN-LEVEL TOPOLOGY OVER THE EXISTINGSEVEN-LEVEL TOPOLOGIES

In this section, the seven-level topology is compared to other existing classic and advanced topologies in terms of the number of active switches, passive components with the same voltage ratings, and the complexity of satisfying the control objectives of each topology for proper operation. Since seven level topologies use steps equal to Vdc/6 to generate seven level voltage at the output, the base voltage rating used in this section for active switches and flying capacitors is equal to Vdc/6 (1 p.u.). The voltage rating for the active switches of this topology is Vdc/3, and the bidirectional active switches equal to Vdc/6, therefore it would have 14 active switches per phase with same blocking voltage. Since the outer FCs voltages should be balanced at Vdc/3, and inner FCs on Vdc/6, this topology has 6 FCs with the same voltage rating. In addition, the voltage balancing of the FCs is the only requirement for proper operation of the converter.

As stated before, the number of components for a seven level classic topology is significantly high. A seven-level NPC would have 12 active switches, 30 diodes per phase. In addition, a seven-level NPC has 5 neutral points that need to be balanced to have equal voltage stress on the active switches, which makes the controller too complex. A seven-level FC converter has similar challenges; 12 active switch, and 15 FCs per phase that need to be balanced at the desired voltages. Seven-level CHB topology, is still in use in industrial applications due to its modularity, and convenient maintenance and control. The CHB topology consists of three cascaded cells of H-bridges.

The big disadvantage of a CHB topology is bulky and expensive phase shifting transformer to provide isolated DC sources for each cell. Each cell has a dclink equal to Vdc/6, so each active switch voltage rating is as the voltage of the dc link for each cell. 12 active switch and 3 dc-link capacitors are used per phase. In addition, using active front-end rectifier for regenerative applications adds to the complexity and cost of the converter. Hence, this seven level topology has less manufacturing cost in comparison to seven-level CHB,

since it does not require any isolated dc sources, and a phase shifting transformer.

A hybrid seven-level converter is proposed, which is a combination of four-level NPC, and three-level FC converter connected in series to generate seven-level voltage at the output. The voltage rating of active switches is equal to Vdc/6, since FCs voltages' are balanced at Vdc/6, and the dc link capacitor voltages are balanced at Vdc/3. Therefore, there are 14 active switches, two FCs per phase, which has the same number of active switches in compare to this seven-level topology in this paper. However, there are two neutral points at the dc bus that increase too much complexity into the controller to balance neutral points.

Another seven-level topology is proposed, which is an upgrade from four-level NNPC, however, the voltage ratings of the active switches are Vdc/3 and Vdc/6, which will result in 18 active switches with the same voltage rating per phase, and five FCs with the voltage rating of Vdc/6. A seven-level MMC topology is also presented, which has 24 active switches and 12 FCs per phase. The seven-level topology in this paper has a fewer number of components in comparison to the topologies presented.

Recently, a seven-level Hybrid-Clamped topology has been proposed in which has active switches with the voltage rating equal to Vdc/3 and Vdc/6, and one FC that needs to be balanced at Vdc /6. This topology requires 20 active switches with Vdc/6 voltage rating and 1 FC per phase. In addition, the voltages of two neutral points must be controlled to ensure equal voltage stress on the active switches. Clearly, the number of active switches of the 7-level topology in this paper is less than the 7L-HC.

The summary of the comparison between the seven-level topology in this paper and other existing topologies is shown in Table. 4.1. Since for different voltage level applications, the dc bus voltage changes and different IGBT modules (1.7-6.5 kV) and capacitors with different voltage ratings can be selected, therefore the comparison has been done in two voltage levels; Vdc/6 and Vdc/3.

Table 1 Number of Components in 7-Level Topologies

	7L-CHB [18]	Hybrid-7L [19]	7L-ANNPC [20]	7L-MMC [21]	7L-HC [22]	7L Topology
IGBT (V_{dc}/3)	36	42	30	72	36	24
FCs (V_{dc}/3)	-	6	9	36	3	12
IGBT (V_{dc}/6)	36	42	54	72	60	42
FCs (V_{dc}/6)	-	6	15	36	3	18
Neutral points	-	2	-	-	2	-
Isolated dc sources	9	1	1	1	1	1

As shown in Table 1, in both voltage levels, this 7-level topology has less number of components in comparison to classic and advanced topologies. In addition, the number of neutral points for each topology is shown to demonstrate the complexity of the controllers.

3.2 OPERATION OF THE SEVEN-LEVEL TOPOLOGY

The single-phase diagram of the seven-level topology is shown in Figure 1. This topology is an upgrade from six-level topology proposed. This topology benefits from combining the feature of flying capacitor topology and a Neutral point piloted (NPP) topology. The bidirectional active switch establishes a controllable path to generate more voltage levels, and a current path to charge and discharge the FCs. Proper operation of the converter and equal voltage stress on active switches (Sx1-Sx8) requires balanced voltages of FCs to generate seven-level voltages at the output terminal.

Table 2 The Switching States Of The Seven-Level Converter

Sx_1	Sx_2	Sx_3	Sx_4	Sx_5	Sx_6	Sx_7	Sx_8	V_{cx1} $i_x>0$	V_{cx2} $i_x<0$	V_{cx3} $i_x>0$	V_{cx4} $i_x<0$	V_{xN}	Output Level
1	1	1	0	0	0	0	0	-	-	-	-	V_{dc}	[6]
1	0	1	0	0	0	1	1	C	-	D	-	$\frac{5V_{dc}}{6}$	[5]
1	1	0	1	0	0	0	0	-	-	C	C	$\frac{2V_{dc}}{3}$	[4c]
1	0	1	0	1	0	0	0	C	C	D	D		[4b]
0	1	1	0	0	1	0	0	D	D	-	-		[4a]
1	0	0	1	0	0	1	1	C	-	-	C	$\frac{V_{dc}}{2}$	[3]
0	0	1	0	0	1	1	1	-	D	D	-		
1	0	0	1	1	0	0	0	C	C	-	-	$\frac{V_{dc}}{3}$	[2c]
0	1	0	1	0	1	0	0	D	D	C	C		[2b]
0	0	1	0	1	1	0	0	-	-	D	D		[2a]
0	0	0	1	0	1	1	1	-	D	-	C	$\frac{V_{dc}}{6}$	[1]
0	0	0	1	1	1	0	0	-	-	-	-	0	[0]

C: Charge Flying-Capacitor D: Discharge Flying-Capacitor - : No impact

Cx1, Cx2 must be controlled at Vdc/3, and Cx3, Cx4 require voltage balancing at Vdc /6, where x = a, b, c. Seven-level voltage is generated by 12 switching states

as shown in Table 2. As shown in Table 4.2, there are redundant switching states for level 2, 3, and 4, which is used to balance the FCs voltages. In each switching state, based on the direction of the output current, FCs are either charged or discharged. A controller based on MPC is developed and explained in the next section, which uses redundant switching states to balance the FCs voltages. For instance, There are three distinct switching states to generate level 4, assume that the phase output current is positive, state [4a] discharges Cx1, Cx2 while state [4b] charges Cx1, Cx2 and discharges Cx3, Cx4, and state [4c] only charges Cx3, Cx4.

3.3 MODEL PREDICTIVE CONTROL OF THE SEVEN-LEVEL TOPOLOGY

Due to the development of fast microprocessors, Model predictive control has gained considerable attention in power electronics recently. Easy digital implementation, nonlinearity inclusion, fast dynamic response, simultaneous satisfaction of multi-control objectives without PID controllers, and PWM blocks, are the advantages of MPC which caused its' emergence into the power electronics. The concept of MPC in power electronics is based on the mathematical model of the converter in terms of switching states, and predicting the systems variables' behavior in the future states.

A cost function is used to force the control objectives to track the predefined references, by selecting an appropriate switching state that minimizes the cost function. For the digital implementation of the control method, the discrete mathematical model of the converter is required. The control objectives for the proper operation of this seven-level converter are output currents, and FCs voltages'.

In this section, the control objectives mathematical models are obtained in terms of switching states and converters parameters'. In each sampling time, control objectives values and their references are predicted for the next sample time, and then a cost function is used to select the best switching state that minimizes the error between the control objective values and their references. Kirchhoff's voltage law is applied to the circuit diagram, shown in Figure 4.1, to obtain the phase voltage of the converter in terms of load current that results in,

$$V_{xN} = Ri_x + L\frac{di_x}{dt} + V_{nN} \quad (1)$$

Where; x = a, b, c, and VxN is the phase voltage of the converter respect to the negative dc-link voltage (N). i_x is the output current of the converter. To simplify the equations filter and load resistance and inductance are shown as R and L. VnN is the common mode voltage, which can be obtained as;

$$V_{nN} = \frac{1}{3}\left(\sum_{x=a,b,c} V_{xN}\right) \quad (2)$$

$$V_{xn} = V_{xN} - V_{nN}$$

From (4.1) and (4.2), and first order derivative of the output current (4.3), the discrete mathematical model of the output current in term of phase voltage and converter parameters can be obtained as;

$$\frac{di_x}{dt} = \frac{i_x(k+1) - i_x(k)}{T_s} \quad (3)$$

$$i_x(k+1) = \frac{T_s}{L+RT_s}V_{xn}(k+1) + \frac{L}{L+RT_s}i_x(k) \quad (4)$$

Where k, and k+1 refer to present and next sampling interval, and Ts is sample time. As shown in (4), to calculate the output current (ix (k+1)) in the next sampling interval, the output current at kth instant which is obtained from output current sensors, and phase voltages in (k+1)th instant are required. Phase voltage in (k+1)th is calculated in terms of all switching states, which is a prediction of the phase voltage for the next sampling interval using equation (2). Equation (5) from Table 2 shows the relationship between the output voltage and switching states of the converter where 0 and 1 represent if the switch is OFF or ON respectively;

$$V_{xN} = V_{dc}(S_{x1}) + V_{Cx1}(S_{x2} - S_{x3} - S_{x4} + S_{x6}) + V_{Cx2}(S_{x6} - S_{x5}) + V_{Cx3}(S_{x3} - S_{x2}) + V_{Cx4}(S_{x5} - S_{x4})$$
$$x = a, b, c \quad (5)$$

Where VCx1-4 are FCs voltages obtained from voltage sensors. Therefore, equations (2), (4), and (5), with the obtained output currents obtained from current sensors, will result in the output current in next sampling interval in terms of all switching states. To predict the FCs voltages in the next sampling interval, the following equations are used. First order derivation is used to obtain the discrete-time mathematical model for the FCs voltages';

$$i_{Cxi}(k) = C_{xi}\frac{dV_{Cxi}}{dt}$$
$$\frac{dV_{Cxi}}{dt} = \frac{V_{Cxi}(k+1) - V_{Cxi}(k)}{T_s}$$
$$V_{Cxi}(k+1) = V_{Cxi}(k) + \frac{T_s}{C_{x1}}i_{Cxi}(k)$$
$$x = a, b, c\_i = 1, 2, 3, 4 \quad (6)$$

As shown in equation (6), to calculate the FCs voltages at (k+1)th instant, the FCs voltages obtained from voltage sensors, and the capacitor currents (iCxi) are required. The capacitor currents in terms of switching states can be calculated as;

$$i_{Cx1}(k) = (S_{x1} - S_{x2})i_x(k)$$
$$i_{Cx2}(k) = (S_{x1} - (S_{x2} \parallel S_{x7}))i_x(k)$$
$$i_{Cx3}(k) = (S_{x2} - S_{x3})i_x(k)$$
$$i_{Cx4}(k) = ((S_{x2} \parallel S_{x7}) - S_{x3})i_x(k) \quad (7)$$

The references for the control objectives, which are the output currents and FCs voltages, are predefined. As mentioned before reference for VCx1 and VCx2 is Vdc/3, and for VCx3, and VCx4 is Vdc/6. Since the dc-link voltage is constant, the references for FCs voltages do not require prediction for the next sampling interval. The output currents references are user-defined, and are predicted for the next sampling interval by Langrage extrapolation as follow, where the user-defined output current reference is i*x

$$i_x^*(k+1) = 4i_x^*(k) - 6i_x^*(k-1) + 4i_x^*(k-2) - i_x^*(k-3) \quad (8)$$

The goal of the controller is minimizing the error between the predicted control objectives and their references. Therefore, a cost function is used to select the switching state that minimizes the error between the output current and their references and FCs voltages references and their actual values. Since there are 12 switching states, as shown in Table. 2) to generate seven-level voltages at the output terminal, in each sampling time, all the possible switching states (123) are examined by the cost function and the best switching state which minimizes the cost function is selected and applied during next sampling interval. When the best switching state is selected, then the gate signals corresponding to this switching states will be extracted from Table 2 and then applied to power switches of the inverter.

$$CF = \sum_{x=a,b,c} \left[i_x^*(k+1) - i_x(k+1) \right]^2 +$$
$$wfcap \sum_{x=a,b,c} \left\{ \sum_{i=1}^{4} \left[v_{Cxi}^* - v_{Cxi}(k+1) \right]^2 \right\} \quad (9)$$

Where wfcap is the weighting factor. As the current control and FCs voltage balancing have equal importance for the proper operation of this topology, the weighting factor is calculated in terms of the rated output current and capacitor voltage references to compensate the difference in nature of the control objectives. The following equation is used to calculate the weighting factor;

$$wfcap = \frac{i_{o,rated}}{V_{cap,ref}} \quad (10)$$

The block diagram of the developed control method based on MPC is shown in Figure 2. The developed control method is convenient to implement on digital controller platforms, and both control objectives are satisfied simultaneously. In the next section, the converter start up is explained, and the experimental results in the next section demonstrate the effectiveness of the developed control method along with the proper operation of the seven-level inverter.

3.3.1 Flying Capacitors Pre Charging and Converter Start-up

There are various methods for pre-charging the flying capacitors using either independent control or auxiliary circuit in the literature since it is an important task in order to avoid damaging the active switches and components in the converter circuit. The different methods for pre-charging the FCs can be used depending on the application. For the presented seven-level topology, it can be assumed that when the dc-link capacitors getting charged slowly through either an auxiliary circuit or using upstream inductor of the transformer, the FCs will be getting charged proportionally, which means that there will be equal voltage stress on the active switches. This can be done by using an R-L load during increasing the dc-link voltage until the dc-link is reached to the required value, and FCs are balanced at their desired value. Simulation has been done in MATLAB/Simulink environment, as shown below, which shows the FCs voltages, and output currents and voltage. As it can be seen the FCs are getting charged while the dc-link voltage increases, and there is no overvoltage or current to damage the switches.

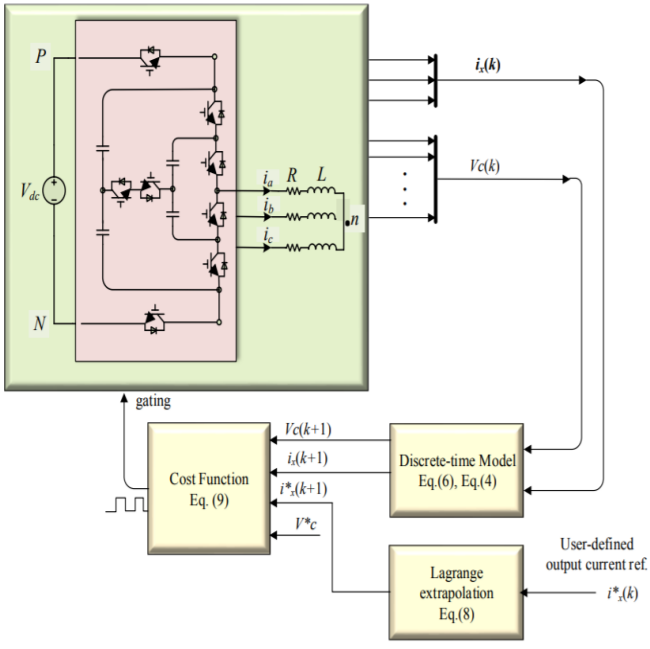


Figure 2 Finite control set Model predictive control strategy for the seven-level converter

3. MATLAB SIMULATION RESULTS

The proposed system is executed in Matlab and the figures show the results of them. The Figure 3 shows the seven level output voltage with modulation index 0.95.

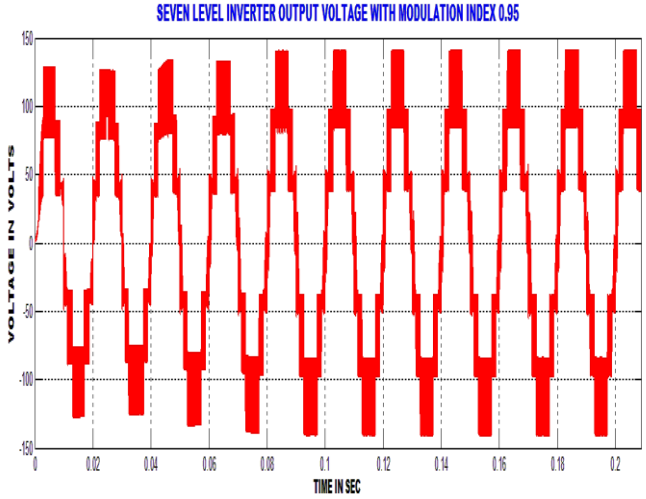


Figure 3 Seven level voltage waveform with M.I = 0.95

The THD is reduced by increasing the DC link output voltage utilization. The FFT analysis of the seven level output voltage waveform with modulation index 0.95 is shown in the below figure 4.

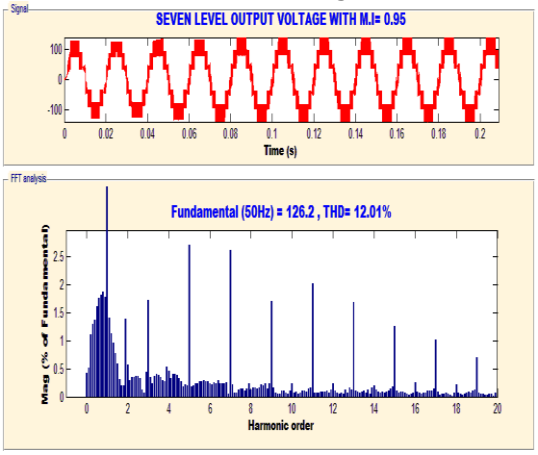


Figure 4 THD waveform with M.I = 0.95

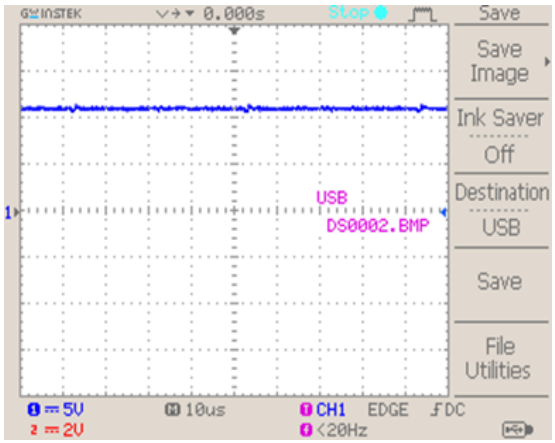


Figure5 Input DC voltage waveform in the capacitor 1

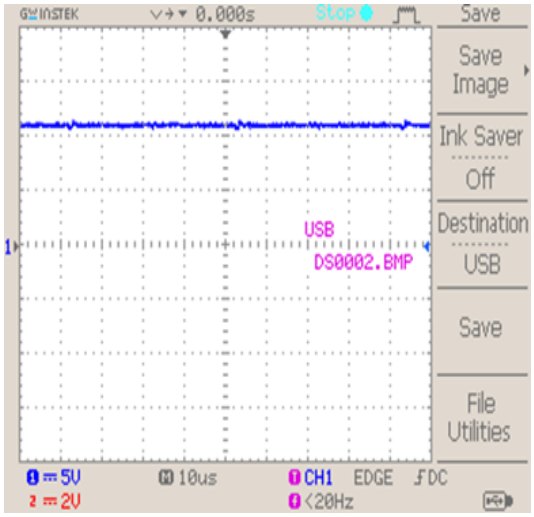


Figure 6 Input DC voltage waveform in the capacitor 2

The capacitor voltages are given to the reduced switch MLI topology. The Figure 7 shows the inverter voltage waveform with modulation index 0.95

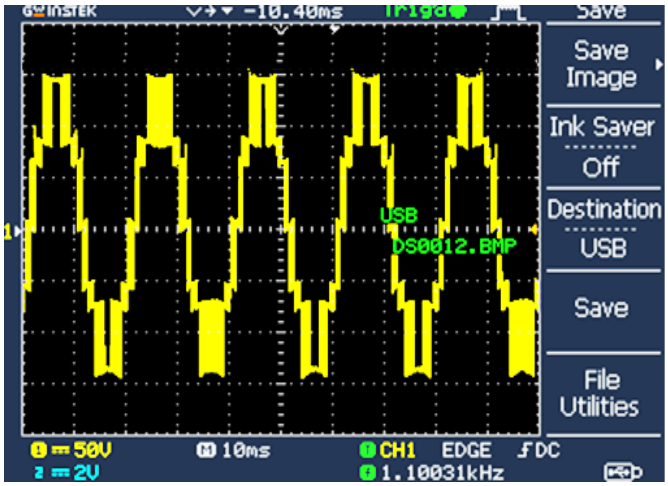


Figure 7 Seven level inverter voltage waveform

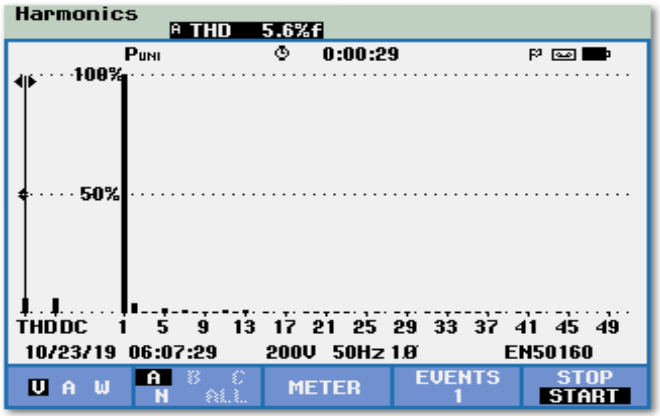
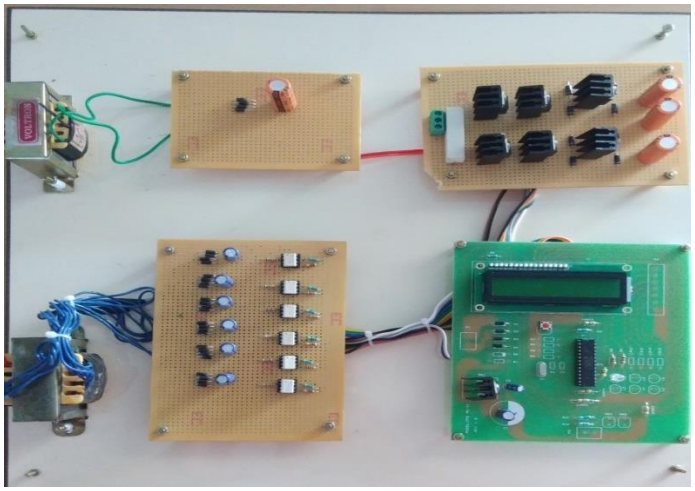


Figure 8 THD waveform of proposed multilevel inverter with filter for M.I 0.95

3. CONCLUSION

Two modified T-type legs are derived from conventional T-type topology. The modified T-type inverter leg can exhibit one switching stress less compared to the T-type leg and also does not require bidirectional switches. Reduction of one switching stress per leg is achieved by increased current sharing through device, as compared to T-type inverter. The output voltage levels of the modified T-type inverter leg cab be increased by addition of H bridged cells at top and bottom. Multiphase multilevel systems can be realized by either leg A alone or leg B alone or all possible combinations of leg A and leg B. A single-phase seven-level inverter formed by the two modified T-type legs is studied using PD carrier based modulation scheme to produce a near sinusoidal voltage at the ac side. High switching frequency operation of each inverter leg produce three level PWM voltage on the AC terminal so that, seven-level output voltage is generated to the load of the proposed inverter. The presented single phase five level topology is found superior with respect to component count and total voltage stress rating.

MODEL OF SEVEN LEVEL VOLTAGE SOURCE INVERTER



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