SPI IMPLEMENTATION WITH LOGIC BIST USING VIVADO IDE

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Abstract - *The target of this project is primarily to structure and implement the Logic Built-In-Self-Test module for Serial Peripheral Interface (SPI) as CUT and test the design. Testing VLSI chips are tedious job because of increasing complexity by expanding exponential progression of nano- technology. Built-In-Self-Test is an essential technique that allows a system to test itself which avoids Automated Test Equipment (ATE) costs and does efficient testing. In this task, BIST structure is implemented and actualized for a SPI. Simulations are performed on the BIST based SPI design. To install a BIST design, additional equipment is required which creates arbitrary test design continuously; it gives less time contrasted with a remotely applied test example considered as Circuit under Test (CUT) and assists with efficiency. In this project SPI (CUT) is simulated and tested individually on vivado.*

Key Words: VLSI, BIST, Serial Peripheral Interface, ATE, Circuit Under Test, vivado.

1.INTRODUCTION

SPI protocol is a Serial Peripheral bus Interface which transfers the data in serial synchronous format, it is a bus interface which is very widely used in communication platform between microcontroller and peripherals such as Shift registers, Analog to Digital Converters , Digital to Analog Converters , Static RAM etc., It is full duplex single master multi slave based interface. The data will be synchronized according to the clock edge (raising edge or falling edge) while transmitting from master to slave and vice versa. This paper concentrates on the 4 wired SPI interfaces which is clock, Chip Select, MOSI, MISO[1].

In the past few years, technology is increasing rapidly and the size of IC chips in VLSI industry is decreasing day by day and the incorporating new features in the small chip is a hectic work and beyond that the testing part is very crucial in any kind of circuit. A small test problem can cause a whole device failure and it can also cause whole version failure which can take billions of amounts. So, DFT (Design-For-Testability) became a preferable technique to decrease area overhead and work efficiently.

Built In Self-Test is an approach for a system to test itself concept taken from Design for Testability model, This concept makes a simple and effective testing to reduce cost of ATE(Automatic Test Equipment) and reduce the reliability upon external testing process and also reduces the complexity. BIST is an unique feature in DFT test techniques where it self-test and consumes less overhead with most approximate results and contain only few blocks in the design which are Random pattern generator, Response analyzer etc. [2]

This paper represents an approach of designing and implementing SPI protocol with Built In Self-Test capability. Using external equipment for testing costs a billions of amount. Therefore, to reduce the cost as well as providing a specified testability with high performance BIST is developed which has much lesser blocks and modules for less complexity. BIST requires less power while testing compared to other testing equipment's.

2. SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is a General Purpose serial synchronous communication interface which is mostly used for short distance information interchangeable purposes, Motorola created the SPI port in 1980's to utilize it in their microcontroller families. The SPI is mostly utilized for the correspondence data exchange between microcontrollers (master) and peripheral devices (slave).The slave performs shifting operation

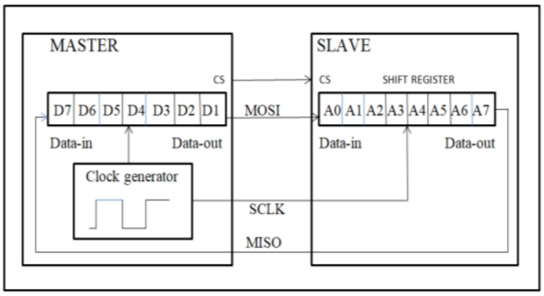


Fig 1: SPI architecture

Fig 1 represents a simple master slave communication process and it shows a 4 wire SPI device, with four signals which are:

1. Chip Select (SC)

2. Serial Clock (represented as SCLK)

3. Master Output slave Input (represented as MOSI)

4. Master Input slave Output (represented as MISO)

Chip Select is present in the SPI master phase where we can select any desired slave and we can establish a connection with the slave and transfer the information, there can be one or more chip select options where we can establish connection with one or more slaves and can transmit the data continuously without interrupting another slave transmission process. Serial Clock is present in the SPI master, where the transmission of the information is synchronized with this serial clock with continuous flow of transmission takes place. Master Output Slave Input (MISO) and Master Output Slave input (MOSI) is present in both master as well as slave. Where if MOSI is enabled, then the master will send the data to slave, If MISO is enabled then the master will receive the information sent by the slave and slave.

A couple of parameters called clock polarity (CPOL) and clock phase (CPHA) decide the edges of the clock signal on which the information are driven and inspected. Every one of the two boundaries has two potential states, which considers four potential blends, which are all contradictory with each other. So a master/slave pair should utilize a similar boundary pair esteems to impart. In the event that numerous slaves are utilized that are fixed in various designs, the master should reconfigure itself each time it needs to speak with an alternate slave.

Specifications of SPI protocol are:

Number of wires used	: Four (4)
Maximum speed	: 60Mbps
Mode of transmission	: Serial
Maximum number of masters	: 1
Data rate per length	: 250 Megabits per second @ 0.1meter
Maximum number of slaves	: Theoretically unlimited
Data paths	: 2
Status Registers	: 2 (miso,mosi)
Control Register	: 1 (CS)
Data bits	: 8 bits(3-16).[1]

3. BUILT IN SELF-TEST

Built-In-Self-Test (BIST) is a plan method where a circuit can test itself. This method can be effectively utilized in different circuits like logic blocks and multipliers etc. The fundamental idea of BIST is to add additional equipment to the chip for test age and reaction assessment it is done on chip with extra equipment overhead[3].

There are a couple of outer pins to control BIST

Input pin: TEST CONTROL (TC)

Output Pin: GOOD/BAD

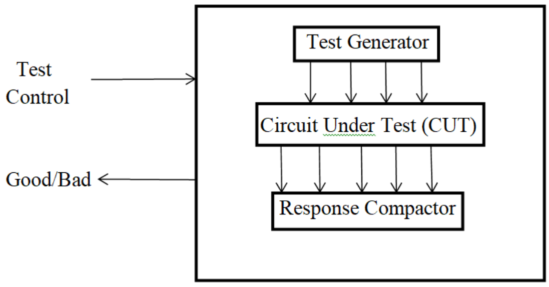


Fig 2: BIST heirarchy

BIST has three important blocks through which the self-test can be obtained. They are: Test generator, Circuit Under Test (CUT), Response analyzer.[2]

3.1 Test pattern generation

Test pattern generator produces a sequence of test patterns and supply it to the Circuit Under Test (CUT), The actual idea of producing these test patterns is to test CUT under different inputs and capture the output thus, we can get every possible fault point tested. To produce these test patterns we used a linear feedback shift register (LFSR) which is widely used as pseudo random pattern generators in many applications. The higher the test patterns we supply, the higher the fault coverage we can achieve. It is based on Shift Register which consists a feedback path that is linear (composed or XOR gates)

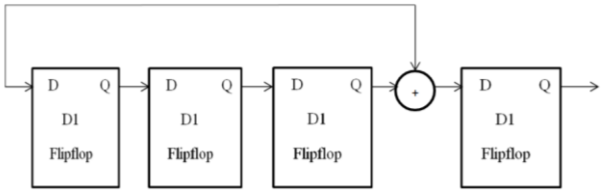


Fig 3: linear feedback shift register

LFSR does not have any external input, once we load it with the initial seed and generate clock, it will run in autonomous way and generates patterns continuously. Considering the characteristic polynomial, it will generate the random patterns accordingly and simultaneously until it reaches the maximum sequence length i.e., For n inputs, m sequence will be (2^m)-1 [4]

3.2 Circuit Under Test (CUT)

This segment is tested under BIST module is started. If the mode is normal, serial inputs primary inputs are fed to the SPI module and the outputs are collected as primary outputs. If the controller selected test mode, then the test patterns are generated and the outputs are fed to the response

3.3 Response analyzer

Test response compaction is a procedure which radically lessen n number of pieces response and it can't understand the initial qualities additionally there will be loss of information. Colossal volume of information in CUT response prompts to produce somewhere in the range of 5 million irregular examples, If CUT has 200 yields it for all intents and purposes prompts around 5 million*200= 1 billion piece responses .For serial input compactor, Serial Input Signature Register(SISR) is used and for parallel input response analyzer an Multi Input Signature Register(MISR) is used. SPI produces data of serial bits, thus we use a SISR as a response compactor [3].

4. BUILT IN SELF-TEST WITH SPI

This structure contains a test controller, multiplexer, test pattern generator, CUT, response analyzer, comparator. BIST controller initiates the process, it decides whether the structure is going through normal or test mode. If the test controller selects to collect data through normal mode, it sends 0 to the selection line of the multiplexer, thus multiplexer sends the serial data to CUT and collected output at PO

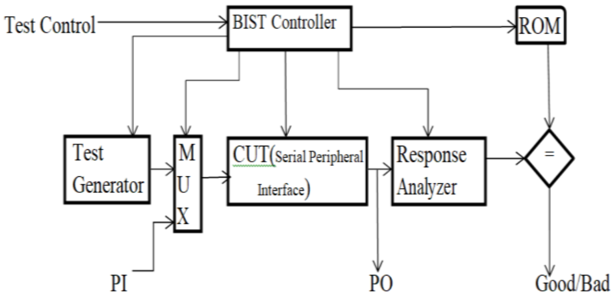


Fig 4: BIST with SPI implementation

In test mode, BIST controller sends 1 to the selection line of the multiplexer, thus multiplexer sends the test patterns data is applied to CUT and the output of the CUT is sent to the response compactor which further forms a signature and compares it with golden signature stored in ROM. If the data received by the response analyzer is wrong then circuit may contain fault [2].

5. RESULTS

Implemented and obtain simulation results for SPI module, Linear feedback shift register test patterns, multiplexer, comparator and BIST with SPI normal mode as well as test mode.

5.1 SPI Module simulation results

Initially SPI interface module is developed and implemented and observed the results that the data we are sending to a particular address is shifted out (slave performs shift operation) when we read the data from the same particular address

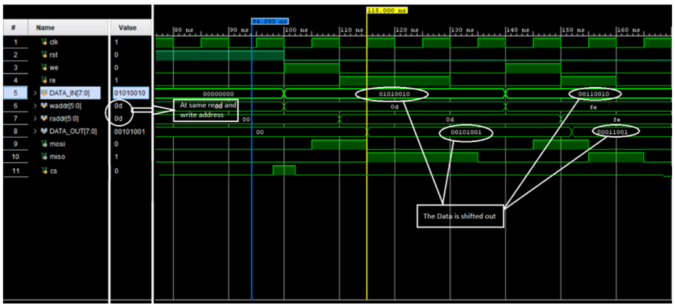


Fig 5: SPI simulation results

Simulation results are captured in vivado 2018.2 version tool and synthesized design is generated. Fig 5 represents the simulation results of serial peripheral device. This data out is stored as golden value to compare with BIST mode.

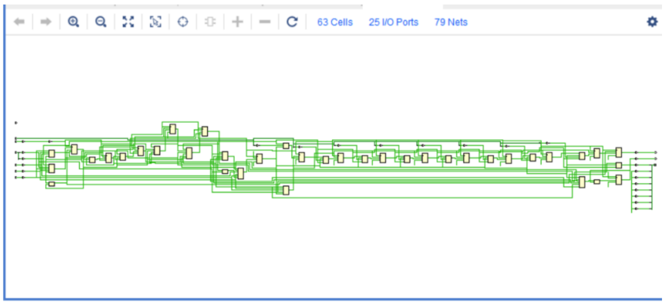


Fig 6: Synthesized design of SPI

5.2 BIST with SPI Module simulation results

First a linear feedback shift register is implemented since we have 8 bit data so, we can generate 255 test patterns through LFSR.

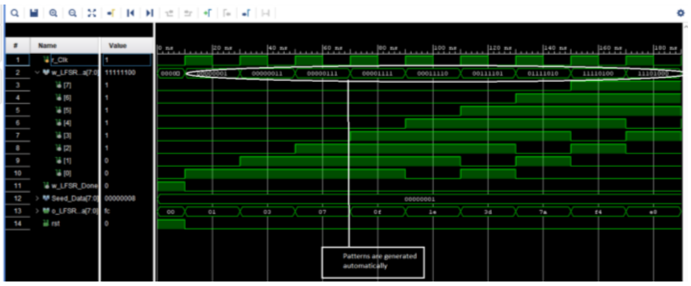


Fig 7: LFSR

A multiplexer is used to select the process is done in normal mode or test mode, the simulation results of the multiplexer is shown in Fig 8.

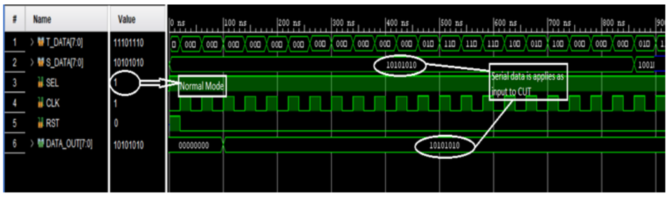
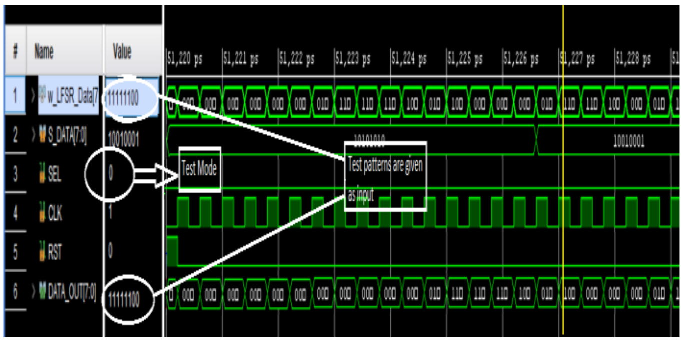


Fig 8: multiplexer in normal mode

Fig 8 shows that, in the normal mode, primary inputs are supplied to the CUT.



Test Mode

Test patterns are given as input

Fig 9: Multiplexer in test mode

Fig 9 shows that test patterns are applied to CUT in test mode.

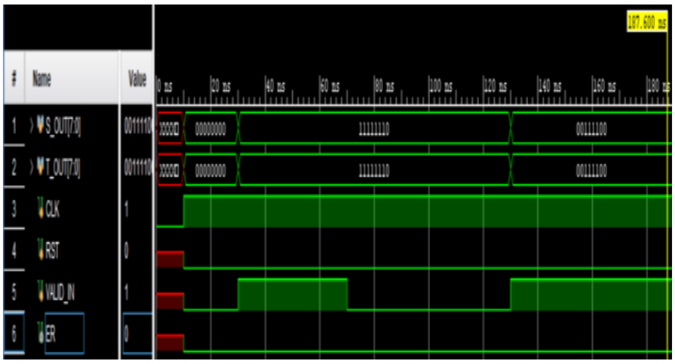
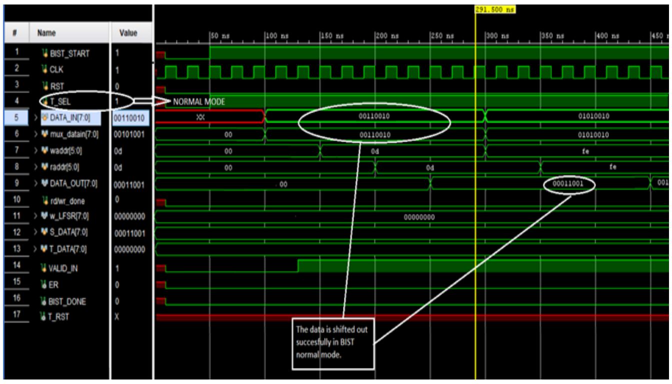


Fig 10: Comparator simulation results

Comparator compares the data to the golden signature stored in the memory and determines whether CUT is working without error or not.

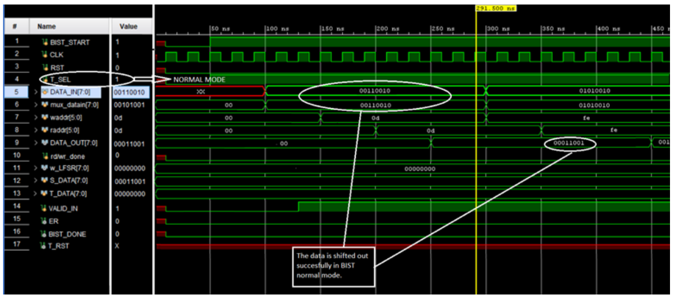


NORMAL MODE

The data is shifted out succesfully in BIST normal mode.

Fig 11: Normal mode simulation results

In normal mode, CUT just functions same as an individual SPI module where the data is shifted out and returns to the master.



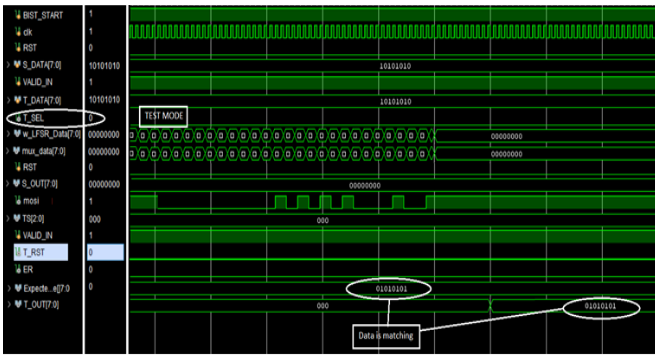
NORMAL MODE

The data is shifted out succesfully in BIST normal mode.

Fig 12: BIST mode simulation results

In BIST mode, patterns are applied to CUT and the results are compacted through the response analyzer then it compares with the golden signature and determines error free circuit.

An another data sequence is also sent with another characteristic polynomial test patterns to obtain the results and Fig 13 resembles it



TEST MODE

Data is matching

Fig 13: BIST mode with data sequence-2

Synthesized design of BIST module is generated through vivado IDE.

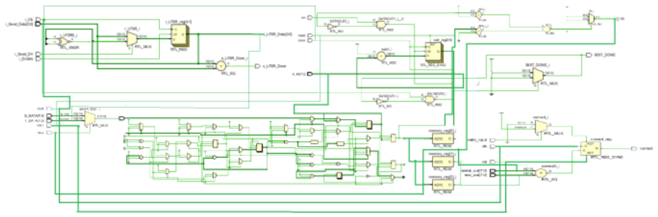


Fig 14: RTL schematic of BIST module

6. CONCLUSIONS

A Circuit under Test (CUT) is developed and made that circuit as self testable circuit. The Serial Peripheral Interface module which is a CUT for BIST is simulated and the results, validate the working as well as a Logic BIST is implemented and in BIST mode values are compared with the golden signature.

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