International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 08 Issue: 08 | Aug 2021 www.irjet.net p-ISSN: 2395-0072

Comparison of various Techniques of 1-bit Full Adder in Cadence 90nm Technology

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Abstract - *Digital circuits have a most common component called as full adder which performs operations of arithmetic such as summation and subtraction. This paper compares as well as analyzes and calculates evolution of different full adders which are constructed using various logic styles. These full adders are analyzed based on power consumption and delay. Here CMOS, Hybrid CMOS, PTL, 10 SERF and 10T GDI are presented. The width of NMOS is 120nm and that of PMOS is 240nm respectively in cadence 90nm technology. 10T SERF and 10T GDI which are included here are the two full adders which are most popular design of full adder. It consists of minimum transistor count as well as less delay and low power when compared with previously constructed full adder designs. The implementation is done in cadence virtuoso. Comparison of these full adders based on power and delay is the major objective. The results and experimental values of power, delay, propagation delay and capacitance are shown in tabular form at the last part. The final full adder which results in less power and delay is further extended to Arithmetic Logic Unit as one of its application.*

Key Words: **Full adder, Power, Delay, 10T SERF, 10T GDI.**

1.INTRODUCTION

Many applications of VLSI use common operation known as arithmetic operation. This arithmetic operation mainly operates two binary numbers addition and calculates it sum. Therefore, full adder is a most significant component of arithmetic circuits which performs summation of numbers and gives sum at its output. Previously these applications were largely focused on area and cost instead of power. Nowadays due to advanced devices and portable devices such as laptops and mobile phones, there is a demand of power to be increased. Such portable devices require high speed along with low consumption of power. But devices which are especially portable require power with high battery. It also causes failure in major parts of the silicon which is a mostly used in such devices. This failure in silicon parts is one of the major drawbacks of electronic devices. Very high amount of cost packaging is required to construct such devices in order to control the levels of heat to consume less power.within parentheses, following the example. But in most industries of semiconductor, designing such devices which produces low power was very critical. Because along with power there is a need to reduce delay as well.

1.1 28T CMOS

A CMOS structure is constructed using equation of adder which is calculated by using full adder of 1-bit truth table. It uses 28 transistors. CMOS is basically a combinational circuit of PMOS transistors and NMOS transistors. These transistors are represented as pull-up and pull-down structure, where pull-up transistors which are PMOS produces strong '1' and pull=down transistors which are NMOS produces weak '0'.

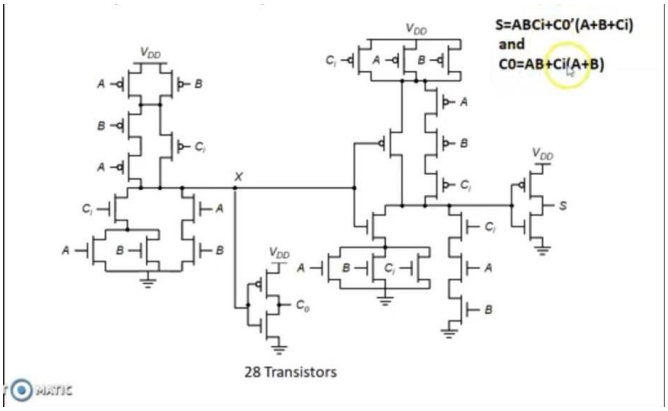

Fig : Block diagram of 28T CMOS

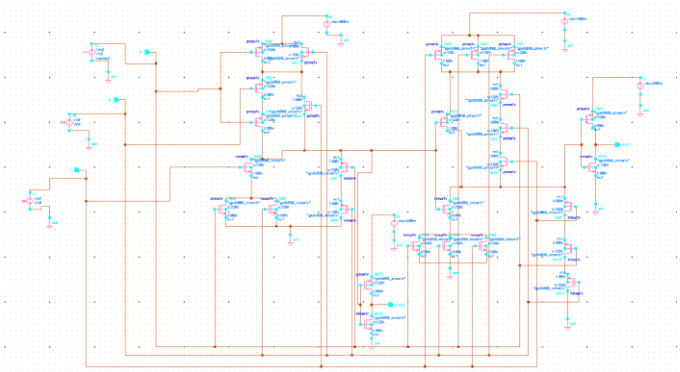

Fig : Schematic of 28T CMOS

1.2 Hybrid CMOS

The Hybrid CMOS uses many types of logic styles, especially CMOS in order to produce a circuit which gives higher efficiency which is as shown in Figure below.

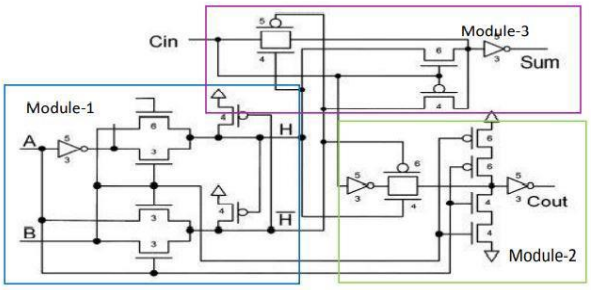

Fig : Block diagram of Hybrid CMOS

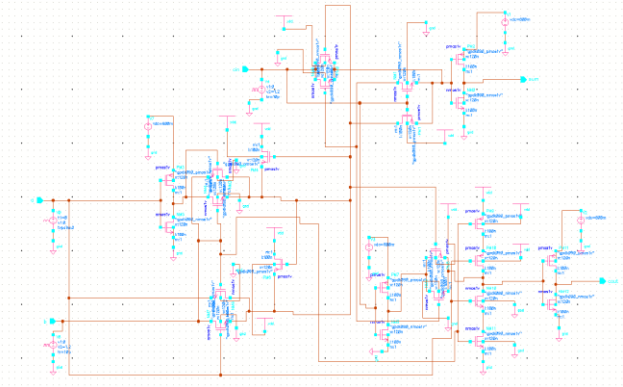

Fig : Schematic of Hybrid CMOS

1.3 Full Adder using PTL Logic

Many families of logics which are implemented according to the circuit which are integrated and signified by Pass Transistor Logic (PTL). The pass transistor logic which is mainly designed to construct various logic gates reduces the transistor count by eliminating the redundant transistors. The Pass Transistor Logic adder is as constructed in figure below and it consists of 20 transistors.

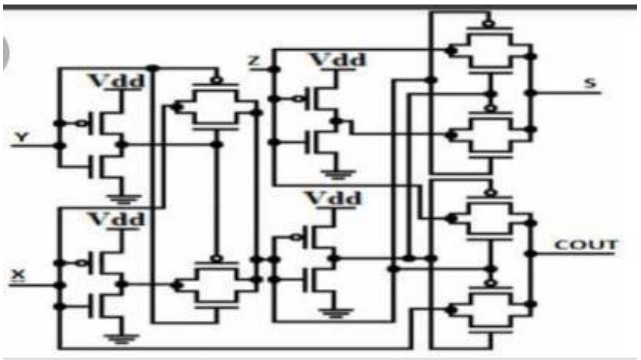

Fig : Block diagram of Full Adder using PTL

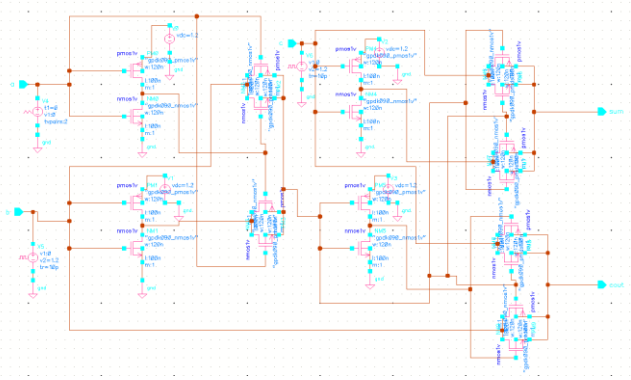

Fig : Schematic of Full Adder using PTL

1.4 10T SERF

This Static Energy Recovering Full Adder design logic is implemented by using two gates which are XOR gates and XNOR gates, by adjusting the delays and propagation delays of output gate. There is unavailability of ground path in the design, and therefore the power consumption gets reduced in this logic design. The charge is reused by control gates and stores load in capacitance. This is an advantageous and efficient design in order to store energy.

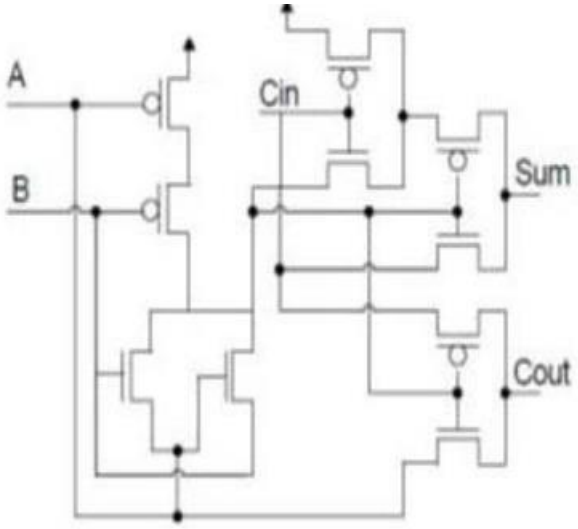

Fig : Block diagram of 10T SERF

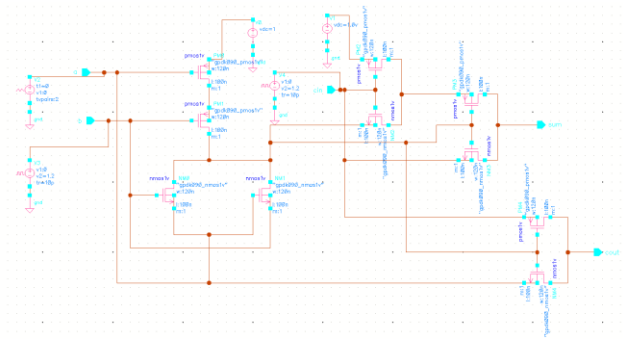

Fig : Schematic of 10T SERF

1.5 10T GDI

The primitive cell of GDI has some similarities with CMOS logic. GDI has an input of three terminals. The P node signifies PMOS transistor, N node signifies NMOS transistor and G is the gate terminal. The difference between CMOS structure and GDI structure is that, both of PMOS and NMOS transistors in GDI are connected to their diffusions. Gate is the common terminal for PMOS transistor and NMOS transistor. The figure below shows the basic cell of GDI, in which the terminal of body is connected to the diffusions in order to reduce the effect of body of the logic.

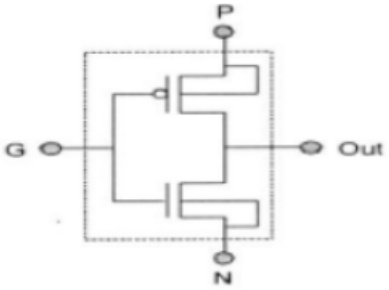

Fig1 : Basic GDI of Cell

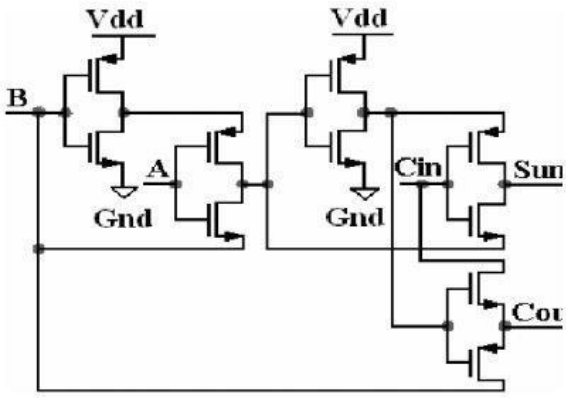

Fig : Block diagram of 10T GDI

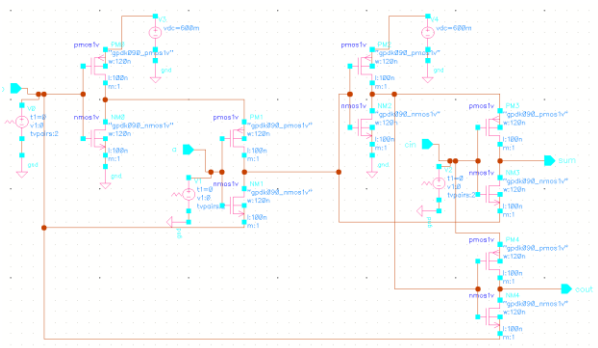

Fig : Schematic of 10T GDI

2. RESULT

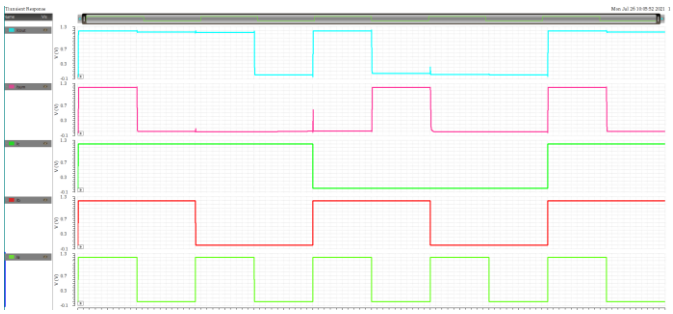

Fig : Transient response of 28T CMOS

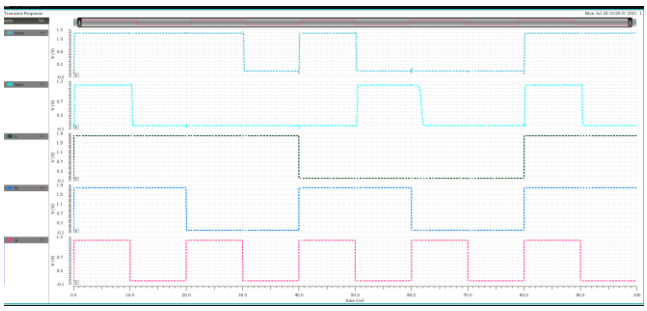

Fig : Transient response of Hybrid CMOS

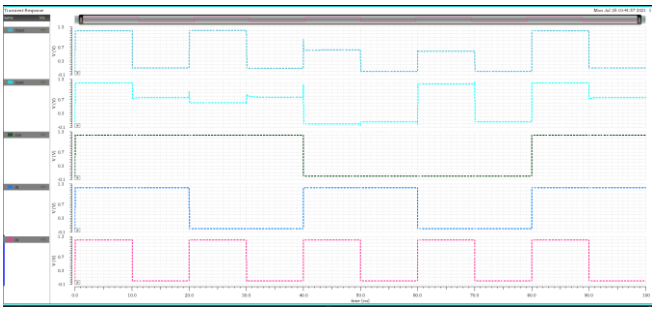

Fig : Transient response Full Adder using PTL

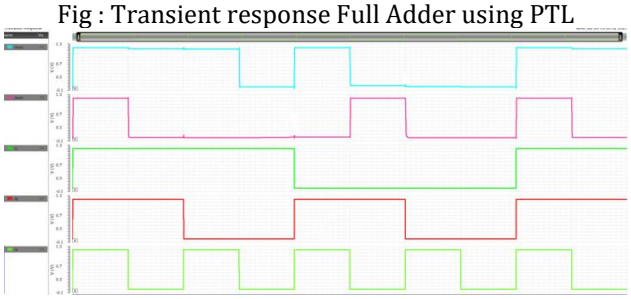

Fig : Transient response of 10T SERF

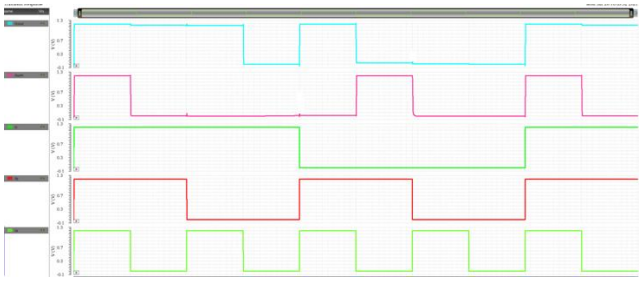

Fig : Transient response of 10T GDI

Table -1:

	CMOS	Hybrid CMOS	Pass Transistor Logic (PTL)	10T SERF	10T GDI
Number of Transistors	PMOS = 14 NMOS = 14 Total = 28	PMOS = 10 NMOS = 11 Total = 22	PMOS = 10 NMOS = 10 Total = 20	PMOS = 5 NMOS = 5 Total = 10	PMOS = 5 NMOS = 5 Total = 10
Power	720.2 uw	600.6 uw	554.8 uw	500.5 uw	456.2 uw
Delay	40.01 ns	30.09 ns	20.09 ns	19.05 ns	10.09 ns
Propagation Delay	0.0383 ns	0.0125 ns	0.00955 ns	0.00528 ns	0.00215 ns
Capacitance	0.996 pf	0.711 pf	0.395 pf	0.274 pf	0.127 pf

Table : comparison of power, delay, propagation delay and capacitance

3. CONCLUSION

The implementation of five types of full adders using various logic styles are been constructed in 90nm cadence technology. The comparison is done between C-CMOS, PTL, Hybrid CMOS full adder and new adder logics which are 10T SERF and 10T GDI full adder. 10T GDI and 10T SERF which are the recently designed full adders consists less number of transistors, when compared with previous designs. Due to the usage less transistors these full adder results in reduced switching activity and area. A broad comparison of all the designs will show the gradual improvement in power dissipation, delay. By making use of this design of full adder of GDI logic an attempt has been made to design the low power less transistor Arithmetic Logic Unit (ALU), since full adder is the fundamental unit of ALU.

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