International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 09 Issue: 10 | Oct 2022 www.irjet.net p-ISSN: 2395-0072

A Comparative Analysis of Vedic multiplier with Array and Wallace Tree multiplier using Cadence

Sheethal S Rokhade[1], Dr. Kiran V[2]

[1]*MTECH 1st year, Dept. of ECE, RV College of Engineering, Karnataka, India*
[2] *Associate Professor, Dept. of ECE, RV College of Engineering, Karnataka, India*

Abstract - *Among the main difficulties in VLSI design in recent years has been power dissipation. In DSP blocks, multipliers are the primary causes of power loss. This project proposes effective architectures for 4-bit unsigned binary multipliers, including the Wallace Tree Multiplier, Vedic Multiplier, and Array Multiplier. The cadence 180nm technology was used for this implementation. In this design, multiplier circuits are effectively optimized in terms of area and power by first designing transistor level schematic circuits and then creating the test symbol. The implementation is made up of combinational parts such 1-bit Full Adders, AND, XOR, Half Adders, and Inverter Circuits. The circuit analysis is done in terms of performance parameters like power consumption and transistor count. According to the analyses, the array multiplier's transistor count and power consumption were found to be 554, 7.457mw, the Wallace Tree multiplier, 500, 7.522mw, and the Vedic multiplier, 464, 7.443mw.*

Key Words: **Multiplier, Power Dissipation, Array Multiplier, Vedic multiplier, Urdhva Triyagbhyam, Wallace Tree Multiplier, Full Adder, Cadence Virtuoso Tool**

1. INTRODUCTION

The difficulty of power consumption in VLSI design is one of the most important. The power consumption of the circuit increases as chip complexity and transistor density do. Since it pulls more current from the power supply, higher power consumption increases chip temperature and has a direct impact on how long portable devices' batteries last. High temperatures compromise the functionality and dependability of circuits, necessitating increasingly sophisticated cooling and packaging techniques. In most digital signal processing (DSP) systems and most VLSI applications, multiplier is one of the fundamental hardware building components. A multiplier is frequently used in DSP applications such as spectrum analysis, digital filtering, and digital communications. Due to the fact that a large number of contemporary When designing DSP applications for compact, rechargeable batteries systems, power dissipation becomes a key consideration. Costly multiplications slow down the operation. The effectiveness of various computer problems is frequently determined by the speed at which a multiplication operation may be done.

1.1 Array Multiplier

An effective design for a combinational multiplier is an array multiplier. Using the "add and shift" technique, this multiplier multiplies using the conventional add and shift operation. Combinational circuits that form the product bit all at once can be used to multiple two binary values with a single micro-operation, making this a quick method of doing so since the only delay is the time it takes for the signals to travel through the gates that make up the multiplication array. Consider two binary values A and B with m and n bits each for the array multiplier. An array of m*n AND gates generates mn summands simultaneously. n(n-2) FA , n HA , and n2 AND gates are needed for the n X n multiplier. Additionally, the worst-case delay in an array multiplier would be (2n+1) td. The optimal number of components are used and more power is consumed by an array multiplier, but the delay is higher. Additionally, the area is increased due to the need for more gates, making the array multiplier less efficient. Consequently, despite the high hardware complexity, it is a quick multiplier.

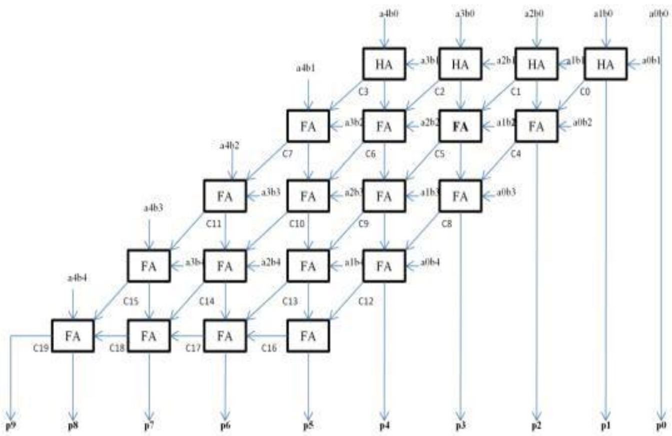
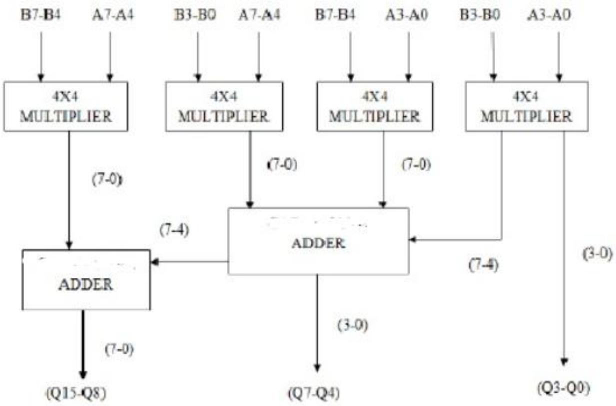


Fig 1: Block Diagram of 4 x4 Array Multiplier

1.2 Vedic Multiplier

Based on the Vedic multiplication formulae, the Vedic multiplier (Sutra). The multiplication of two numbers has always been done using this sutra. A multiplication formula that can be used in any and all multiplication situations is known as the Urdhva Tiryakbhyam (UT) Sutra. The format of the multiplication is "Vertically and crosswise," which is how the term "UT" is literally translated. Throughput is obtained parallel with the use of a revolutionary notion called UT. With the help of the UT algorithm, which is described in fig.2, partial products are generated and their summation is acquired. Because it uses fewer resources than other conventional processes, it can operate at higher frequencies with less strain on the processors. In comparison to other multipliers, the Vedic Multiplier based on the UT technique has the advantage that area and gate delay increase at a constant rate as the number of bits increases. It is therefore effective in terms of power, time, and space.



1.2. Wallace Tree Multiplier

A Wallace tree is a practical optimum design technique for building a circuitry that multiplies two numbers. Wallace trees are renowned for having the fastest calculation times when employing carry-save adders to combine numerous operands into two outputs. The Wallace tree and Dadda multipliers, which are two well-known fast multipliers in comparison to the array multiplier, were also demonstrated by other researchers. The Wallace tree, however, promises the smallest total delay. The Wallace tree's multiplication process begins by multiplying each argument's bits by each argument's bit. Different weights are carried by the wires depending on where the multiplied bits are placed. The number of partial products will then be reduced to two by layering full and half adders. Finally, the wires will be grouped into numbers and added using a carry look ahead adder.

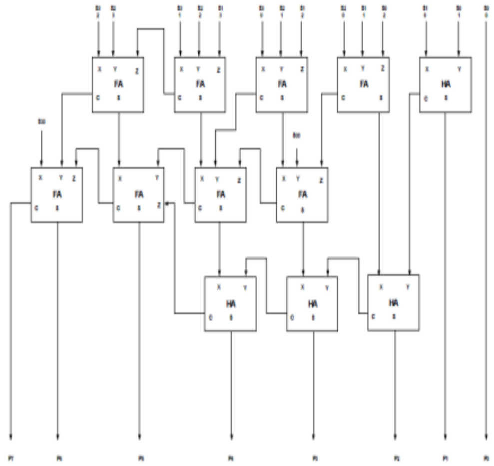


Fig 3: Block Diagram of 4 x4 Wallace Tree Multiplier

2. PERFORMANCE ANALYSIS

Table -1 Transistor Count Associated with Different Multipliers

Name of Multipliers	Transistor Count
Array multiplier	554
Vedic multiplier	464
Wallace tree multiplier	500

Table -2 Power Dissipation Associated with Different Multipliers

Name of Multipliers	Power Dissipation (Uw)
Array multiplier	745.7
Vedic multiplier	741.3
Wallace tree multiplier	752.2

Table -3 Delay Associated with Different Multipliers

Name of Multipliers	Delay (nsec)
Array multiplier	34.04
Vedic multiplier	27.9
Wallace tree multiplier	31.96

3. SUMMARY

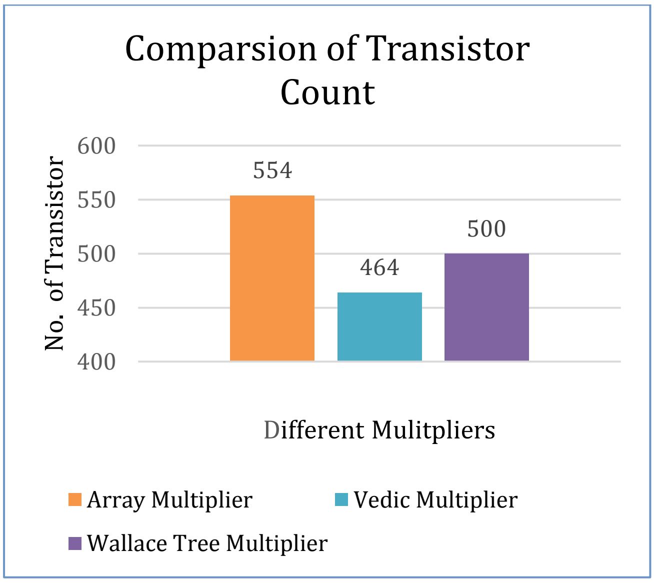


Fig 4. Comparsion of Transistor Count associated with Array,Vedic and Wallace Tree Multiplier

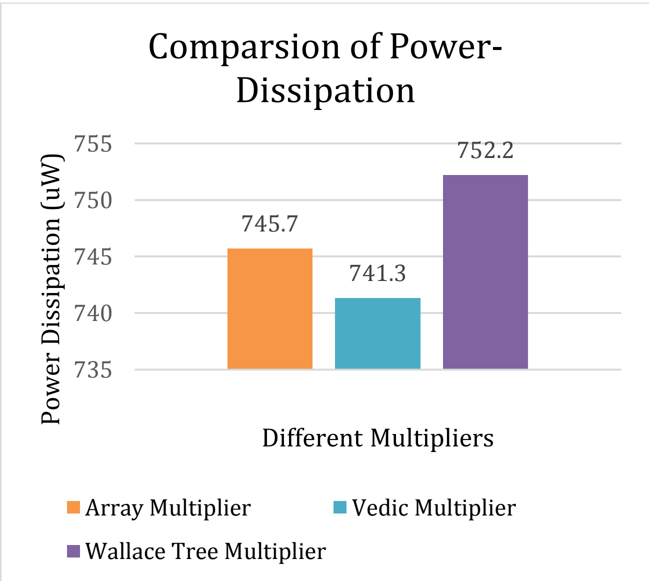


Fig 5. Comparison of Power Dissipation associated with Array, Vedic and Wallace Tree Multiplier

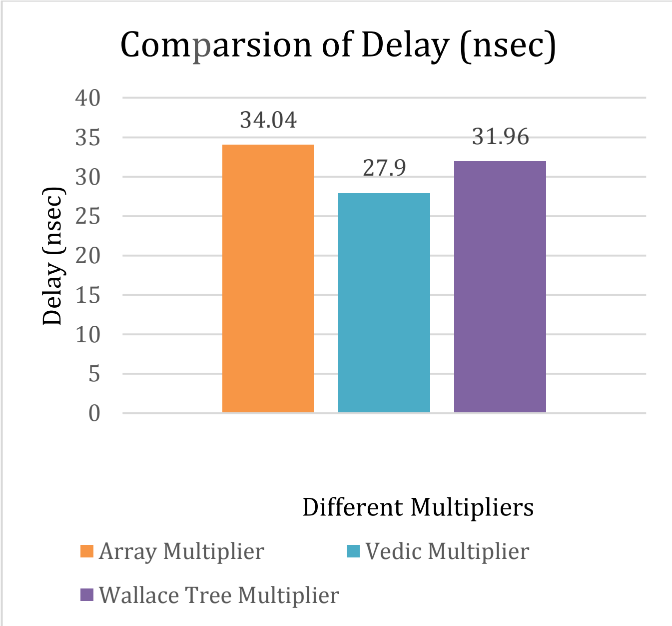


Fig 6. Comparison of Delay associated with Array, Vedic and Wallace Tree Multiplier

The article's main objective is to compare three different multipliers: the array multiplier, the vedic multiplier, and the Wallace tree multiplier. According to the specification, these multipliers are frequently used in a wide range of applications, so they were chosen for comparison. The 180nm cadence technique is utilized to imitate the operation of multipliers. The findings of the multiplier analysis and comparison are tabulated above.

Overall, Comparing all multipliers, the Vedic multiplier uses fewer transistors. Because space is one of the factors that influences a circuit's complexity, Wallace tree multipliers and arrays consume little space and exhibit few variations. A system's productivity is significantly impacted by how much power it consumes .According to the multipliers taken into account, Vedic emerges as the multiplier with the lowest power usage, whereas Wallace tree multiplier has the highest power consumption (752.2Uw) of the multipliers considered (741.3uW). Currently, when assessing the system performance, processing speed is taken into consideration.

3. CONCLUSIONS

Four of the above-discussed multipliers are compared in this section using a variety of performance metrics. The simplest multiplier in terms of circuit complexity and size is the basic array multiplier, which uses the add-and-shift technique to multiply numbers slowly. Based on the results of the study mentioned above, it can be said that, of all the multipliers, the Wallace tree multiplier accelerates the accumulation process due to the employment of carry save adders, but it has the disadvantage of having complicated circuitry that takes up the most space. The simulation's outcomes closely match what was predicted. The design of the multiplier architectures is primarily focused on maximizing their area and power. Transistor count and power usage are just two examples of the factors that are used to evaluate the performance of the various multiplier circuits.

In comparison to the Array Multiplier and the Wallace Tree Multiplier, the Vedic Multiplier is the best multiplier in terms of area, power utilisation, and speed.

REFERENCES

[1] Pradeep Kumar Kumawat, Gajendra Sujediya" Design and Analysis of 8x8 Wallace Tree Multiplier using GDI and CMOS Technology," International Journal of Advanced Engineering Research and Science (IJAERS), 2017, pp. 2349- 6495.

[2] B. Lamba and A. Sharma, "A review paper on different multipliers based on their different performance parameters," 2018 2nd International Conference on Inventive Systems and Control (ICISC), 2018, pp. 324-327, doi: 10.1109/ICISC.2018.8399088.

[3] Immareddy, S., Sundaramoorthy, A. A survey paper on design and implementation of multipliers for digital system applications. Artif Intell Rev 55, 4575–4603 (2022). https://doi.org/10.1007/s10462-021-10113-0

[4] Savita Nair and Ajit Saraf, " A Review Paper on Comparison of Multipliers based on Performance Parameters," International Conference on Advances in Science and Technology (ICAST) , 2014, pp. 6-9.

[5] V. Rajmohan and O. Uma Maheswari, "Low Power Modified Wallace Tree Multiplier Using Cadence Tool," World Engineering & Applied Sciences Journal, 2016 ,ISSN 2079- 2204, pp. 1-10.

[6] M Naresh and B Suneetha, " Design of Low Power Full Adder Based Wallace Tree Multiplier Using Cadence 180nm Technology," , International Journal of Innovative Research in Science, Engineering and Technology (IJIRSET), 2017, pp.8401-8409.

[7] Dr. Savita Sonoli, Sahana Desai, "Design and Implementation of 4x4 Vedic Multiplier using Cadence," International Journal of Engineering Research & Technology (IJERT)), 2020, pp. 732- 735.

[8] G. C. Ram, Y. R. Lakshmanna, D. S. Rani and K. B. Sindhuri, "Area efficient modified vedic multiplier," International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2016, pp. 1-5.

[9] N. R. Mistri, S. B. Somani and V. V. Shete, "Design and comparison of multiplier using vedic mathematics," 2016 International Conference on Inventive Computation Technologies (ICICT), 2016, pp. 1-5, doi: 10.1109/INVENTIVE.2016.7824870.

[10] G.Ganesh Kumar and V.Charishma, “Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques”, Int. Journ. of Scientific and Research Publication, vol. 2, March 2012