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Design and Analysis of a Full Subtractor using Various Design Techniques

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Abstract - *With the development of VLSI design, the integrated chip's gate count is continually increasing, which increases power dissipation and reduces the speed .Therefore, a new architecture that can overcome these limitations needs to be designed. In this paper 1 bit Full Subtractor is designed using various methods and most feasible solution is suggested. The designs have been simulated using Cadence Virtuoso 180nm CMOS technology. Using two XOR gates and 2:1 Multiplexer (MUX) to design a Full Subtractor circuit has turned out to be the most practical design for a full subtractor. It uses 58 transistors uses 42.58uW of power, and propagation delay of 29.45ns making it the most optimized design in comparison to all other methods.*

Key Words: Full Subtractor, Multiplexer, Cadence Virtuoso, CMOS technology, propagation delay

I. INTRODUCTION

As CMOS technology advances towards the nanometer by scaled-down devices. Initially, the main concern for a VLSI design engineer was to reduce the circuit parameters such as area, cost, performance and reliability whereas power consumption was considered next. However, in recent years, electricity usage has been given equal weight to all other factors. Low power consumption is a key component in developing the right solution. To lower the heat generated by the circuit, power degeneracy must be reduced.

The most important requirement is to identify the source of power loss and take necessary action to address it by utilizing proper methodology and technique that can produce the best results.

In order to achieve maximum efficiency in terms of transistor count, delay, and power consumption, the aim is to modify the basic structure of the existing subtractor circuit using a variety of methods, and then come to a conclusion regarding the most effective method among the mentioned methods.

The paper is organized as follows: Section II provides a description on the basic structure of a full subtractor. Section III presents the various other full subtractor design which aides in recommending the best full subtractor design that has been optimized. Section IV all of the full subtractor methods mentioned in the paper are compared using the results of various design properties analyses.

Subsequently, section V presents the outcome's conclusion.

II. ARCHITECTURE STUDY

A. Traditional Method

A full subtractor is a combinational circuit that subtracts two bits, one of which is a minuend and the other a subtrahend, while also borrowing the lower minuend bit that was previously adjacent. Three inputs and two outputs make up this circuit. The three inputs A, B, and Bin, respectively, stand for the minimum, minimum subtract, and previous borrow. The difference and output borrow are represented by the two outputs, D and B out. It is designed using the logic gates AND, NOT, OR and XOR as shown in Figure1.Figure 2 represents truth table of Full subtractor.

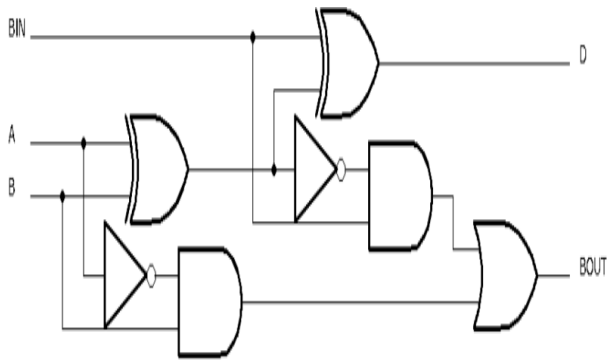

Fig. 1. Conventional FS Circuit

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Fig-2 : Truth Table of FS

Figure 3 represents input and output waveform of a conventional FS where A, B and C in are the inputs and Difference and Borrow are the outputs.

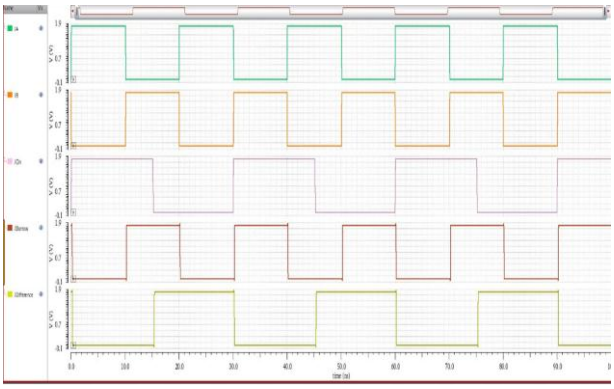

Fig. 3. Input and Output waveform of FS

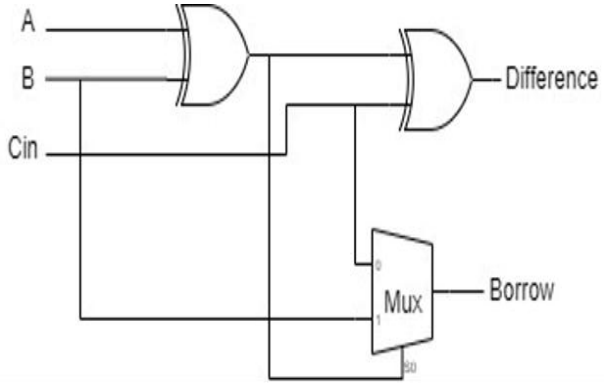

Fig. 4. Method 1 FS

A. Method 1: Using two XOR gates and a 2:1 MUX

The borrow stage of this approach substitutes a Multi-plexer(MUX) with the AND and OR gates. As indicated in Figure 4, the difference stage has been designed using the same two XOR gates as the regular FS.

B. Method 2: Using XNOR Gate and two MUX

Both the difference stage and the borrow step are adjusted in this method. With the use of logic gates and a 2:1 MUX, the Difference stage is produced. Figure 5 illustrates how the borrow step is realized using a 2:1 MUX.

C. Method 3: Using two 4:1 MUX

To further improve the design, both the difference and the borrow stages have been changed in this method. The difference step in method-2 was implemented using a 4:1 MUX in place of the combination of logic gates and gates in this technique. Using a 4:1 MUX, the borrow stage is implemented. The VEM technique is used to realize this design which is shown in Figure 7 and Figure 6 which shows the logical structure of this method.

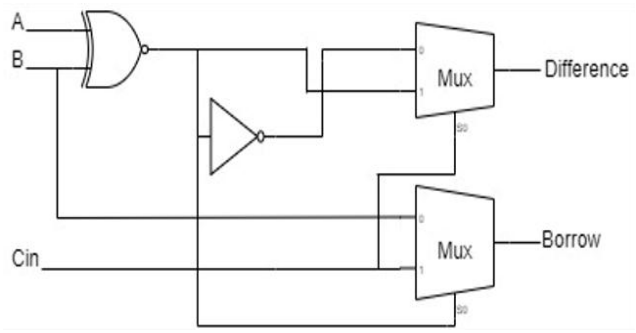

Fig. 5. Method 2 FS

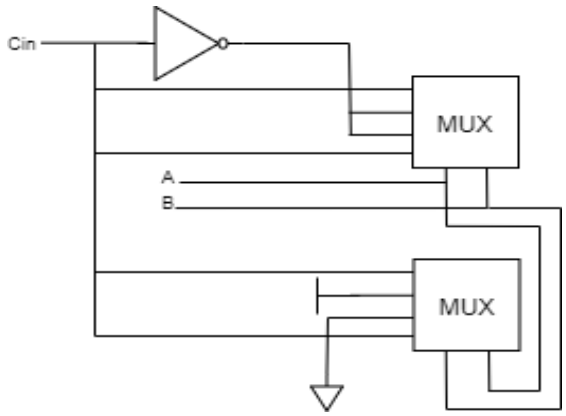

Fig. 6. Method 3 FS

In order to increase the effective size of a k-map Variable Entrant Mapping (VEM) is used and thereby allowing a smaller map to handle a larger number of variables. Therefore, VEM is used to realize the output

equations required for the method 3. As per Figure 7, M1 output variable are the inputs for the first MUX and M2 output variables are the inputs for the second MUX, as shown in Figure 6.

A	B	Cin	D	Bo	Input to MUX	
					M1	M2
0	0	0	0	0	Cin	Cin
0	0	1	1	1		
0	1	0	1	1	$\overline{Cin}$	1
0	1	1	0	1		
1	0	0	1	0	$\overline{Cin}$	0
1	0	1	0	0		
1	1	0	0	0	Cin	Cin
1	1	1	1	1		

Fig. 7. VEM Table for Method 3

The 4:1 MUX is implemented using both CMOS as well as Transmission gate logic. Figure 7 represents 4:1 MUX using Transmission gates where X0,X1,X2,X3 are the inputs and C0,C1 are the select lines of the MUX.

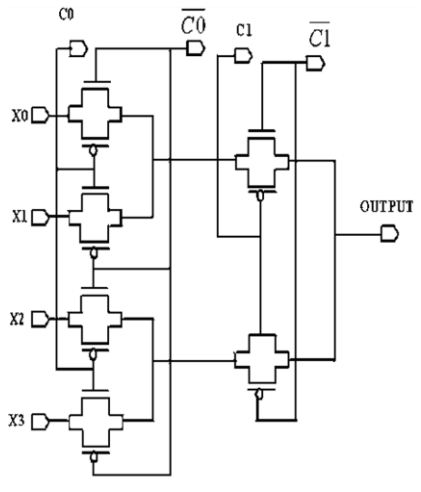

Fig. 8.4:1 MUX using TG logic

III. Result Analysis

The various Full Subtractor methods is simulated on Cadence Virtuoso tool using 180nm technology with a supply voltage of 1.8V. According to the Comparison Table, the Conventional method has the least propagation delay (28.87ns) but the power consumed is the most amongst all the methods (46.21W). The Method 1 design is the most optimized since it uses fewer transistors (54) than the other technique. Method 3b utilizes the greatest number of transistors (62) and has a higher propagation delay (40.23 ns) compared to all other methods therefore making it much slower and less efficient. The graphical representation of comparative analysis of all the method with respect to number of transistors, power consumption, and the propagation delay is shown in Figure 10, Figure 11 and Figure 12.

Methods	Number of transistors used	Power(μW)	Propagation delay (ns)
Conventional Method	54	46.21	28.87
Method 1	52	43.30	31.34
Method 2	58	42.58	29.45
Method 3a (CMOS logic MUX)	62	36.11	38.92
Method 3b (TG logic MUX)	62	41.76	40.23

Fig. 9. Comparison of all the methods

IV. CONCLUSION

This work implements various full subtractor designs and analyses the various design aspects to suggest optimized method. Because less transistors are used in the method 2 FS as compared to all other techniques, it can be concluded that employing two XOR gates and a 2:1 MUX where MUX is designed using CMOS logic results in lower power usage. Therefore, it can be inferred that the most efficient approach to construct an FS that can be integrated into a system's ALU is to use two XOR gates and a 2:1 MUX. The system can be portable and used in energy-efficient applications according to the suggested design.

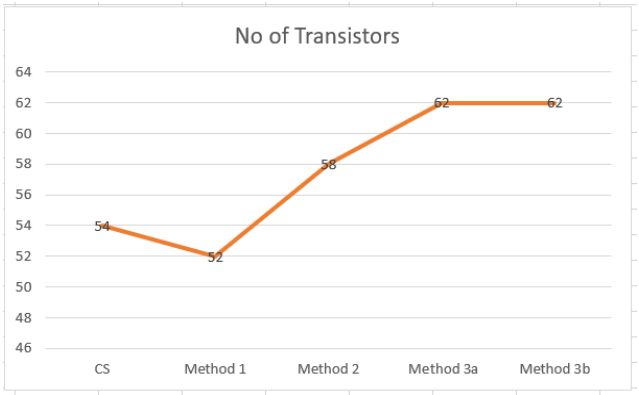

Fig. 10. Transistor Count Comparison of all the methods

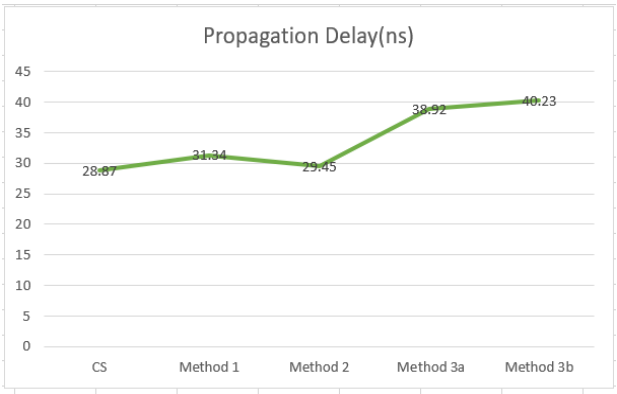

Fig. 11. Delay Comparison of all the methods

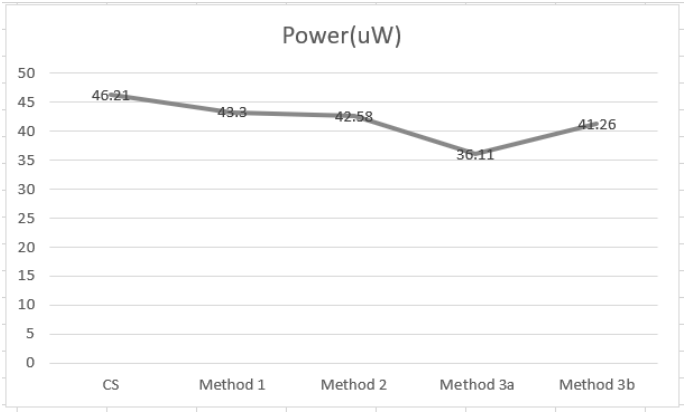

Fig. 12. Power Comparison of all the methods

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