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Performance Study of Transformerless Three-level Inverter for PV System

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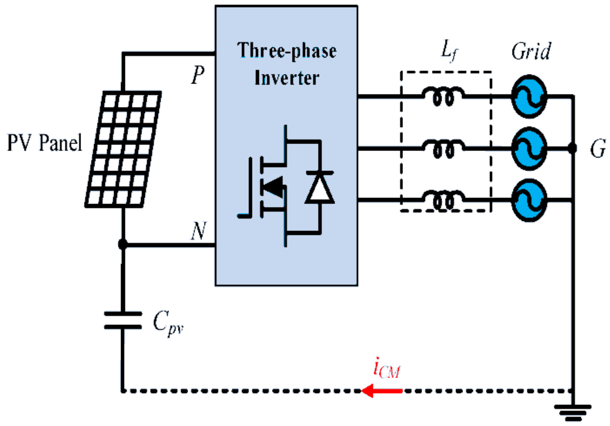
Abstract – *This_study investigates the effectiveness of the Performancea Transformerless Three-Level Inverter in the context of a Photovoltaic (PV) System employed in Building Integrated Photovoltaic (BIPV) systems. The system consists of several components, including a photovoltaic (PV) array, a boost DC_/DC converter, a three-level neutral_-point-clamped_ (_NPC_) inverter, an LC_ filter, and a grid connection. The 3-level NPC inverter is engineered to operate without the inclusion1 of a galvanic isolation transformer. Its current controller is specifically designed to mitigate the occurrence of leakage currents in the common-mode voltage circuits of photovoltaic (PV) systems. A The MATLAB programme was utilised to simulate the prototype1 of a 170.9 kW transformerless three-level inverter incorporating an LC filter. The simulation yielded a total harmonic distortion (THD) of less than 1.59% and an efficiency of 97.6% at the peak export to the local network. The discussion extensively covers the1 simulation and test results.*

Keywords1 PV1; 3-φ1 transformerless1 inverter1; NPC1; boost1 converter1; current 1control1, LC 1filter; maximum power1 point tracking1.

I. INTRODUCTION

In recent times, a considerable number of transformers less Three-level inverters have been developed and widely implemented for the purpose of renewable energy generation, specifically in photovoltaic (PV) systems. In the realm o.f buil.din.g_-integ.r.ated phot.ovolt.aic_ (B.I.P.V) s.ystems, there is a noticeable emergence of _small_-scale P.V_ systems with a capacity of up to 15 kW [1]. In general, these systems need a galvanically isolated, three-phase inverter to change the direct_ current (D.C) voltage from photovoltaic (PV) arrays into_ alternating_ current (A.C) _ volt.a.ge., which is then sent into the utility grid.
notably three-phase Three-level transformerless topologies are the most prevalent way to convert DC voltage to AC voltage in power systems due to their low cost, simplicity, and maturity.

Transformerless topologies' PV array-grid connection without galvanic separation is a drawback. Thus, worldwide organisations have established PV inverter safety standards. Large stray capacitance (CPV) between the PV panel and grid ground is the key safety problem. Figure 1 shows a grid-to-PV panel ground-current route. CMV variations cause leakage current because of excessive stray capacitance between the PV panel and grid grounds. The leakage current passes through the ground and PV array, increasing radiated electromagnetic emissions, current harmonics, losses, and dependability of transformerless, grid-connected PV transformerless inverter topologies. These difficulties need careful leakage current management. In VDE 0126-1-1, leakage current must be less than 300 mA to avoid negative impacts. Reduce the CMV amplitude and frequency or disconnect the PV array from the grid on the DC side of the inverter system to reduce leakage current. In recent years, many methods have been developed to reduce transformerless PV inverter CMV and leakage current in recent years.Problem solved later.
The use of an inverter featuring galvanic isolation presents viable solutions for addressing safety considerations and enhancing the adaptability of voltage and current. However, it is important to note that these solutions may entail substantial weight and cost.



(a)

implications. Line transformers and high -frequency transformers increase power conversion circuit inefficiencies, reducing photovoltaic inverter efficiency [2].

A transformer,less inverter topology can address the restriction. However, compatibility issues with the common-mode voltage and leakage current have caused electromagnetic interference (EMI,) and safety concerns. Single-phase inverters with high switching frequencies are more affected by the above issues [3]. High, ,- ,speed, switching induces d,v,/d,t, and d,i,/d,t,, which cause compatibility issues.

The three-phase inver,ter has similar issues. Thus, the design needs two goals.

To safeguard the PV, array, and lengthen the DC link capacitor's life, reduce the dv,/dt and di,/dt values. The second goal is to reduce current loss through the common-mode, channels that connect the PV, array, to the grid. EMI should also be reduced. The two main issues are lowering the d,v,/d,t and d,i/d,t ratios and optimising the P,W,M switching mechanisms employed by the inverter and boost D,C,/D,C, converter,.

Multilevel inverters reduce device dv/dt, voltage stress. This method adds levels. DC link capacitors can also have a lower vol,tage rating, providing more low-cost options [4]. PV systems, can, eliminate, leakage, current through common,-mode, voltage, circuits using advanced switching modulation [5].

This research offers a Transformer,less Three,- ,level ,Inverter Performance Study for a PV System with an L,C filter for B,I,P,V systems. The suggested current controller operates the new inverter without a transformer for efficient ac,tive, and reac,tive, power. The transformer,less, inverter's new current controller with an L,C filter reduces total harmonic distortion (THD) to less than 5%. PSIM and MATLAB help characterise the common,-mode voltage, leaka,ge current, current controller, and LC filter. The prototype was modelled, using MATLAB software in a 170.9 kW transformerless, three-level Inverter with an LC filter, which showed less than 3% total harmonic distortion (THD,) and 97.6% efficiency,, at peak export to the local network. Reviewing simulation, and test results

II. PHOTOVOLTAIC, THREE,-PHASE, 3-,LEVEL, INVERTER SYSTEM,,

Overall,, System, ,Conf,iguration

Figure 1 shows a transformer,less, three-phase, three,-,level N,P,C inverter setup. Figure 1 shows this configu,ration. The system includes a P,V array, boost D,C,/D,C, converter,, three-level N,P,C, inverter, L,C fil,te,r, and grid. P,V array output voltages range from 513.6V to 630V,D,C,.

The utility grid inverter system outputs 170.9 kW at 380 volts and 50 Hz. Low switching frequencies max,imise system efficiency. D,C/D,C converters switch at 10 k,Hz, while inverters switch at 5 k,Hz.

The 3,- ,level N,P,C inverter can generate Vd,c,, +Vd,c/2, 0, and -Vd,c/2 utility grid voltages depending on switching frequency. An L,C filter reduces vol,tage ripple and T,H,D.

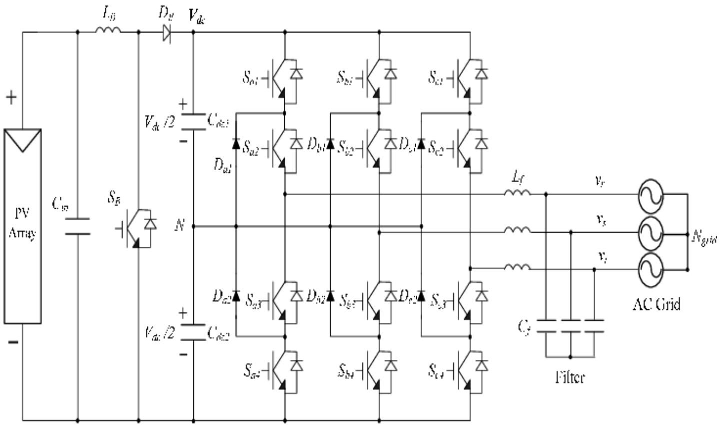


Fig. 1. Overall configuration of a transformerless three-phase 3-level NPC inverter system.

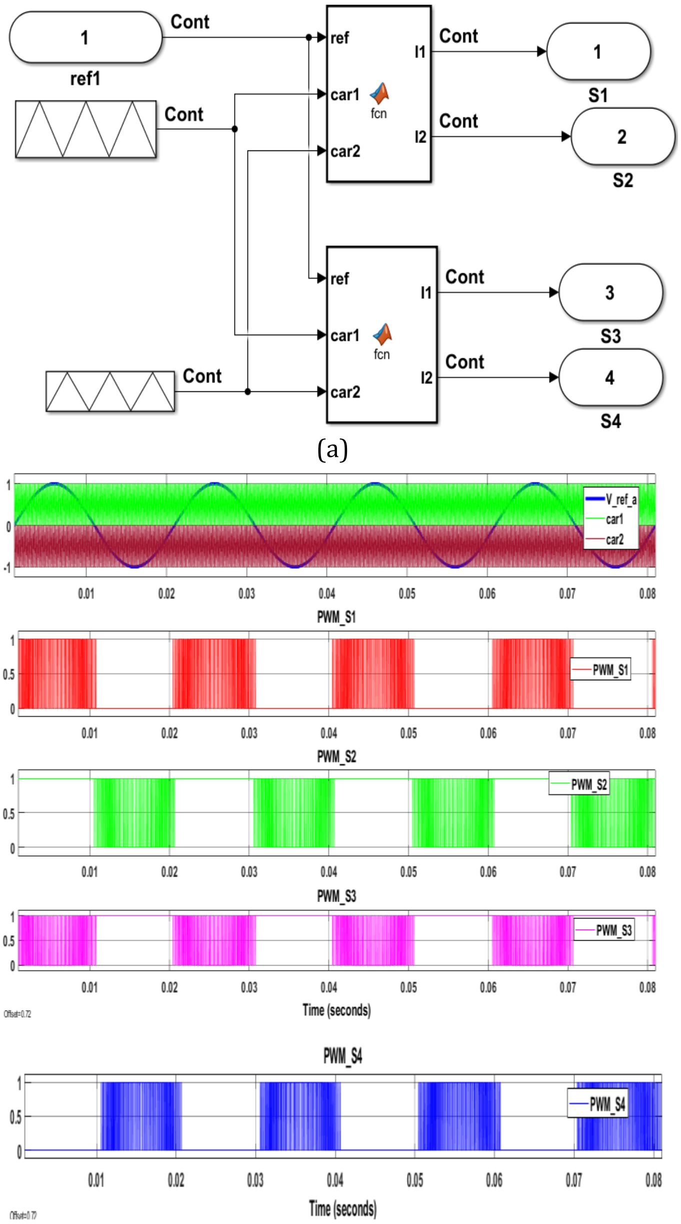
B.PWM Strategy

During zero-sequence switching, stray capacitances and leakage inductances can make the, common,-mode, vol,tage ,loo,p into a reso,nant, circuit, [5–6]. A galvanic connection between, the g,rid ,g,round and the P,V array causes this.

,The inverter is affected by zero-sequence and triple-harmonic currents flowing from the photov,oltaic (P,V) array to the grid via a direct or low-impedance connection. A common-mode, voltage, which is shared by the input photovoltaic (P,V) ar,ray, and the outpu,t gr,id termin,als, can also cause resonance,.

Thus, this resonance can generate a large inverter common-mode current. Thus, such acts can cause system instability, so avoid them.

Pulse, width modulation, (P,W,M) can be used in three-phase neutral-point-cla,mped (N,P,C) inverters in three ways: phase disposition (P,D), phase opposition disposition (P,O,D), and alternative phase opposition disposition (A,P,O,D). Figure 2 shows the PD P,W,M switching scheme. a phase disposition-using limb in a three-level neutral-point-clamped (N,P,C) inverter. The proportional-derivative (PD) method reduces inverter line-to-line voltage harmonic distortion [6]. The D,C,/D,C con,verter's switching frequ,ency is 10 k,Hz to decrease input current disturbance, while the inverter's is 5 k,H,z for system efficiency.



(a)

(b)

Fig.2. The box chart (a) PD PWM switching pattern in a phase leg of Transformerless Three level Inverter for PV System(b).

II. CONTRO,L AN,D DESIG,N OF THREE,-PHASE, 3-LEVE,L NPC INVER,TER WITH LC FIL,TER

A. Control, Sys,te,m

Figure 3 depicts the primary controllers that make up the control system of a g,rid-,connected Transformer,less ,Three,- ,level, Inver,ter, for a Photovol,tai,c (P,V) System. These controllers are a direct current (D,C)- ,side ,controller,, for the boost D,C,/D,C conver,ter and an alternating current (A,C)-side ,control,ler, for the inver,ter,.

Both of thes,e controlle,rs are referred to as primary controllers. The controller for the whole system combines the controllers for th,e li,ne voltag,e at the po,int of commo,n coupling (PCC), the current flo,wing through the inverter, and the grid current that is controlled by the D,C link, vol,tage,.

It is the job of the D,C/D,C converter to keep the regulated D, C ,link, volta,ge, at a level, that is high enough to allow the inverter to function properly. This is accomplished by keeping the link voltage at a level that is high enough. The maximum, power, point, tracking, (M,P,P,T) controller makes use of a perturbation and observation (P&O) approach [7] in order to get the photovoltaic (PV) array to produce the most amount of power possible. This is done in order to maximise the efficiency, of the system,.

The, Max,imum Power, Point, Tr,acking, (M,P,P,T) method is responsible for generating a current reference that is proportional to the boost inductor current at its output. Proportional-integral

(P,I) controllers are used everywhere throughout this specific system, including but not limited to the maximum power, point tr,acking (M,P,P,T) voltage controllers as well as the inductor current controllers.

The control system for the three-level NP,C inverter's major purpose is to efficiently regulate and stabilise, the direct current (D,C) voltage while also ensuring the smooth transmission of ,photovol,taic (P,V)-generated power to the grid and reducing the presence of harmonic currents as much as possible. This is the fundamental aim of the control system. The, current, controller, is run within a d,-q, synchr,onous, frame,, and, all of its variable values are gener,ated, inside a d,-q, coordinate, system,. The findings of the, PI cont,roller must be converted from the coordinate system into phase quantities before the P,W,M switching, pattern can be considered compliant [8]. This conversion must take place before the phase quantity criterion, can be satisfied.

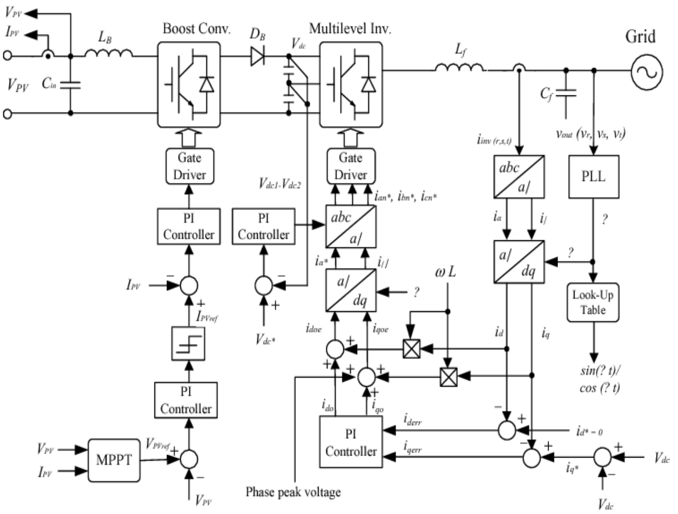


Fig. 3. Control block diagram of a 3-level Transformerless inverter.

B. Current Control.

The existing controller incorporates circuits for controlling both active and reactive power [9]. The present controller is employed to modulate the output power of the photovoltaic system. The controller in a proportional-integral (PI) current loop is responsible for regulating the output current to align with its reference values.

The active power regulation in the Transformerless three-level Inverter for PV Systems involves the measurement and comparison of the output power with the allusion to power. The power error is sent to a proportional-integral (PI) controller, and once there, it serves as the reference for the output current, which is shown by the symbol iq*. The voltage output of the inverter is also measured and subsequently compared to the voltage reference in order to derive the d-axis.

current reference, ID *. In a comparable manner, the mistake is inputted into a PI current controller and subsequently regulated for reactive power through the grid-connected Transformerless Three-level Inverter. The controller's output power is determined by the reference active power and the measured output power of the transformerless inverter. The determination of the gains of the proportional-integral (PI) controller is contingent upon the disparity between the measured voltage and the reference voltage.

The present reference, however, is formulated using a synchronous reference d-q axis frame, which rotates at the same frequency as the grid and is aligned with the d-axis. The voltages for each of the three phases that have been measured are transformed into a synchronous rotating reference frame based on the frequency of the grid.

Also, the result of this proportional-integral (PI) controller is used to make the commands for the inverter to switch the current.

Table 1: Switching table states in a phase leg of the 3-level Transformerless inverter

Operation Modes for phase A(upper) Sa_1&Sa_2	Operation Modes for phase A (Lower)Sa_3 & Sa_4

function [I1 ,I2] = fcn (ref, car1, car2)
signal = zeros (2,1);
if ref >= car1
signal (1) = 1;
signal (2) = 1;
elseif ref < car1 && ref > car2
signal (1) = 0;
signal (2) = 1;
elseif ref < car2
signal (1) = 0;
signal (2) = 0;
end
I1 = signal(1);
I2 = signal (2);
end
	function [I3 ,I4] = fcn (ref, car3, car4)
	signa3 = zeros (2,1);
	if ref >= car3
	signa3 (3) = 0;
	signa4 (4) = 0;
	elseif ref < car1 && ref > car4
	signa3 (3) = 1;
	signa4 (4) = 0;
	elseif ref < car2
	signa3 (3) = 1;
	signa4 (4) = 1;
	end
	I3 = signal(3);
	I4 = signal (4);
	end

The id * and iq * components of the d-q current command are transformed into the ian*, ibn*, and icn* components of the a-b-c current command, respectively. The reference vectors are generated through the use of the space vector modulation algorithm in order to produce the gate signals.

The PI current controller GPI (s) in the d-q reference frame can be defined as follows:

$$K_{PI}(s) = K_P + \frac{K_i}{s} \qquad (2)$$

The symbol Kp denotes the proportional gain, while Ki represents the integral constant. Because the PI controller is built in parallel and doesn't change over time, the gain parameters don't affect the direct and inverse sequence components of the current error [10]. This is due to the decomposition of the PI controller into a parallel structure and the constant nature of the proportional gain parameter (Kp). Hence, It is essential to have a solid understanding of the KP in terms of the accumulation of the proportional gains connected to the already present sequence controller.

In order to achieve dynamic response, the use of a, gr,id vol,tage, feed,-for,ward, loop, is necessary for, the P,I controller.

Howe,ver, it is important to note that this approach has the potential to yield a significantly reduced total harmonic distortion (T,H,D) of, the, discharge cur,rent,. The B,. LC filte,r is a type of electronic filter that uses inductors (L) and capacitors (C) to selectively pass The use of a basic L-filter is a prevalent practise in the mitigation of current harmonics in Transformerless Three,-Level Inverters. The design of the L filter requires a high inductance value to accommodate the line frequency, resulting in a significant increase in cost, as indicated by a reference [11].

Furthermore, there is a potential for a slowdown in the dynamic reaction. As a result, the low-pass filter may be replaced with LC or LCL filters instead, both of which have quite modest values for their inductors and capacitors. It uses an LCL filter, which is characterised by the presence of two inductors, which results in increased size and cost. The effectiveness, cost, loss, weight, and dimensions of a filter may vary depending on its type. This study involves the creation of an LC filter.

Prior to the design of the LC filter (references 12–13), it is imperative to ascertain the maximum amplitude of the ripple alternating current. The side inductance of the Transformerless Three-level Inverter is selected to be 5,% of, the phas,e curr,ent at, its rated power in this particular design. This, guidel,ine posits that the primary constituent of grid current is of a negative nature. As a result, it is necessary for the inductor voltage's fundamental component to exhibit a negative polarity. Hence, the voltage across the inductor can be represented as:

$$V_L = V_{inv} - V_g \qquad (1)$$

The variable VL represents the, voltage, across, the induc,to,r, Vinv denotes the voltag,e output of the inverter, and Vg signifies the voltage of t,he gr,id.

On t,he other han,d, the phase vol,tage of the Transform,erless Three-leve,l Inver,ter exhibits five distinct levels relative to the midpoint, namely Vd,c, V,d,,c/2, 0, -V,d,c/2, and -Vd,c.

In comparison to the grid frequency (f,N), the higher switching frequency (fs) has an impact on the phase voltage. Therefore, it can be stated that the average value of the out,put vol,tage Va,v of the inve,rter remains constant during the transition period Ts. The calculation of the pea,k-to-pea,k v,alue of the fi,lter inductor, cur,rent is deter,mined through the use of the PD PWM switching method.

$$\Delta I_{PP} = 2I_{rpm} = \frac{\frac{V_{dc}}{2} - V_{av}}{L_f} \cdot \frac{d_1}{f_s} \qquad (2)$$

The variables Ip,p and Irp,m are the symbols for the pea,k-to-pea,k value and the ma,x,imum val,ue of the ripple in the fi,lter inductor current, respectively.

The value of th,e, fi,lter, inductance is represented by the letter L, while the duty cycle is symbol,ised by the number d1. During the time period in which 0 is less than t and more than,

L stands for the filter inductance value, while d1 represents the duty, cycle,. Dur,ing the interval where 0,, < ,t, < π,

$$V_{av}(\omega t) = d_1(\omega t)\frac{V_{dc}}{2} \qquad (3)$$

$$d_1(\omega t) = m_a sin(\omega t) \qquad (4)$$

wh,ere, ma is modu,lation index. Hence, the maxi,mum i,nductor current r,ipple I,rpm can be expressed as fol,lows:

$$\Delta I_{rpm} = \frac{V_{dc}}{4L_f\, f_s}[1 - d_1(\omega t)]d_1(\omega t)$$

$$= \frac{V_{dc}}{4L_f\, f_s}[1 - m_a sin(\omega t)]m_a sin(\omega t) \qquad (5)$$

As,suming ma = 1, the m,aximum value of I,rpm is 1/4 at ,π,,/6, 5, π,,/6.

$$L_f = \frac{V_{dc}}{16.f_s \ .\Delta I_{rpm(max)}} \qquad (6)$$

Therefore, the determination of the value of the inductor on the invervter side of the transformerless three-level Inverter was reliant on the switching frequency.

When determining the appropriate filter capacitance, the maximum, power fac,tor fluctuation observed by the g,r,id is assumed to be 5%. The derivation of the total system ,impedance, base value, Z,B, is based on the variation in capacitance.

$$Z_B = \frac{V^2{}_G}{P_{AV/\ \ 3}} \qquad (7)$$

$$C_B = \frac{1}{\omega_N\ .Z_B} = \frac{1}{2\pi F_N\ \ .Z_B} \qquad (8)$$

$$C_{max} = 0.05.C_B \qquad (9)$$

In this context, vG represents the root mean square voltage between the lines, PAv denotes the active power rating, and, N signifies the frequency of the grid. In equation (9), when utilising values exceeding the threshold The actual power f,actor of th,e sy,stem will be lower than the powe,r fac,tor that was projected by a margin of 5%.

The ripple in the current that is carried by the inductor will be magnified if capacitors of an excessively large size are used.

Nevertheless, it is important to be aware that the transformerless inverter is capable of displaying common-mode voltage loops even when switching using pulse width modulation (PWM). As a result, a resonance circuit is formed, and its resonant frequency can be determined by considering the boundary condition between the switching frequency and the control bandwidth. [14]

10. $f_N \le f_{res} \le \frac{f_s}{2}$ (10)

where, fresv is the resonance frequency and is defined as:

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}} \qquad (11)$$

It is imperative to select a switching frequency that is significantly higher than the resonant frequency of the LC filter.

III. SIMULATION AND VERIFICATION

C. Digital Simulation Setup

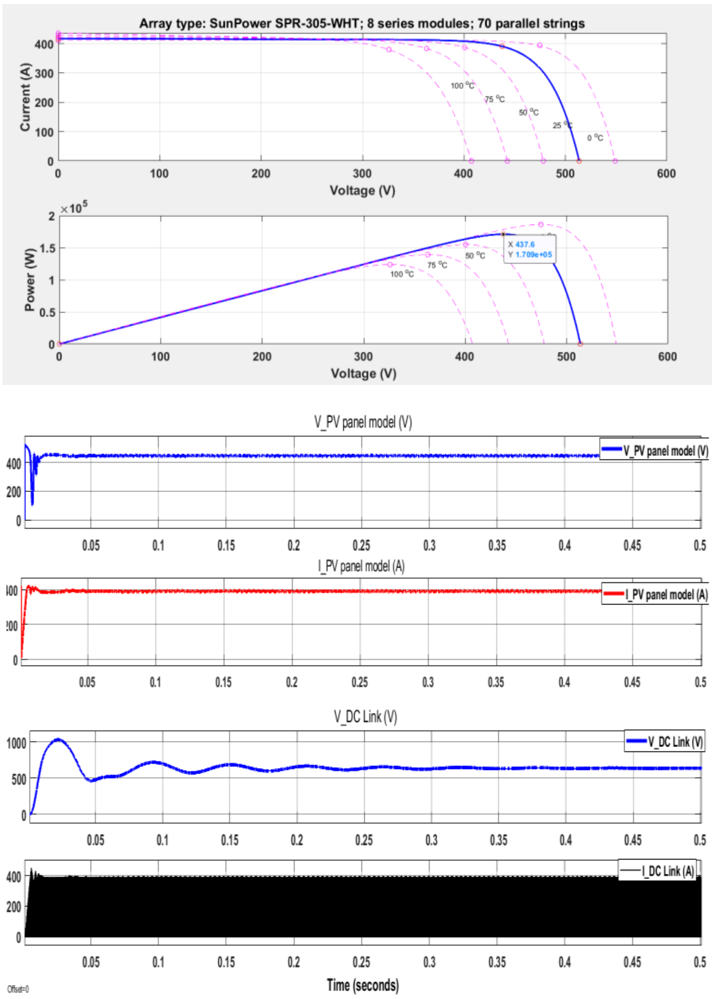
The digital simulation setup is a crucial component in conducting research and experimentation in various fields. It involves the creation and configuration of a virtual environment that mimics real-world scenarios.

In order to conduct After exhaustive analysis of the system, the suggested inverter is simulated using PSIM. The system parameters that were employed in the simulation are detailed in Table 1. Figure 4(a) is a representation of a schematic diagram based on the PSIM software, and Figure 4(b) is an illustration of the waveforms of the output voltage of a 3-level inverter and the line-to-line grid voltage. Both figures are located in the same figure. The output of the 3-level inverter demonstrates five separate voltage levels, which are denoted as Vdc, Vdc/2, 0, -Vdc/2, and -Vdc, respectively. The switching frequency determines whether or not certain voltage levels are present.

Figure 4(c) displays the grid with the rated currents that were put into it. According to the findings of the simulation, the waveform of the injected currents is sinusoidal, and their total harmonic distortion (THD) is around 2.5%.

TABLE 2 SIMULATION PARAMETERS

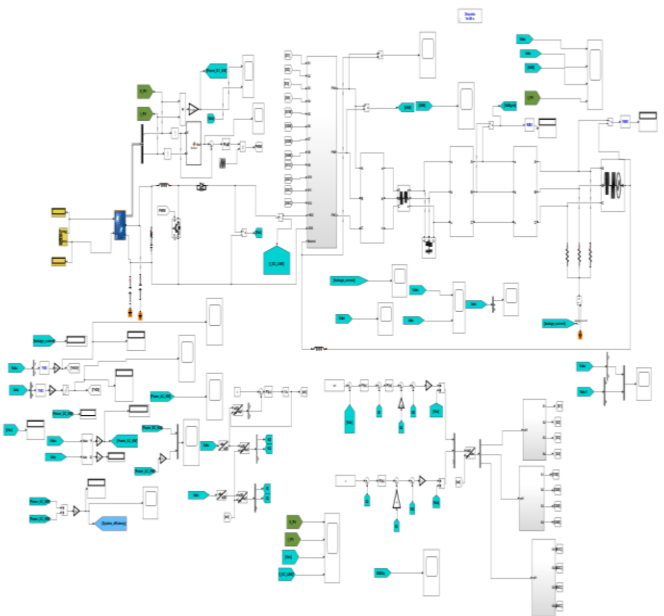
Key parameters	Values
PV Array voltage	514 - 630 Vdc
Grid	50Hz, 3Φ, 380 V(rms)
Nominal Power	170.9kW
PWM carrier frequency_ Inverter	5 kHz
DC-DC converter	10 kHz
LC Filter	4.5mH/ 10µF



(a)

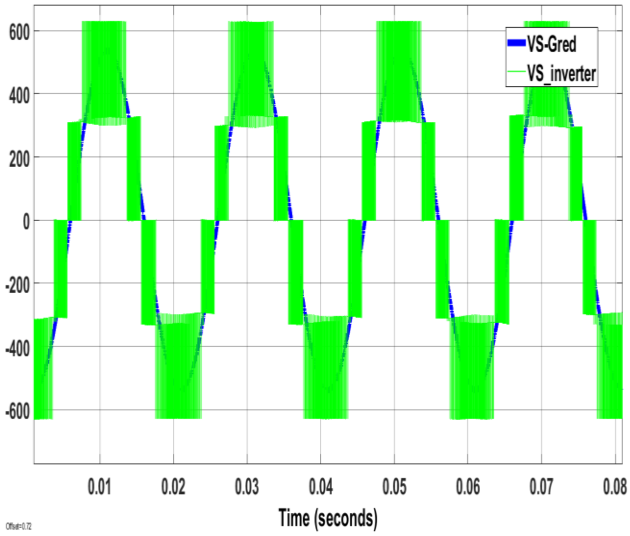
Table 2 shows system parameters. Three-phase rooftop systems have 15 kW power ratings. This study utilised 170.9 kW. The transformerless inverter's DC bus voltage was 650 V if the 3-phase grid was 380 V at 50 Hz. The PV panel structure was 8 series cells with 70 parallel strings for 180 kW of output power and VDC. A simple capacitance model modelled the leakage capacitance (Cearth) between cells and the grounded frame. Depending on climatic conditions and panel construction, it may be 50–150 nF. The simulation used 100 nF for the earth. The real time for one control algorithm procedure determined the sampling time (Ts). The remaining parameters were chosen because 3-phase inverters need them.

the NPC transformerless inverter and PI current controller with SPW modulation results. The two controllers sinusoidally phase the grid currents (unity power factor). PI controller grid current THD is 2.23%. Each controller action produces a distinct waveform for the inverter output line voltages. Since both controllers employ the same MPPT controller, their PV currents are identical. The PI controller clearly controls earth leakage current.

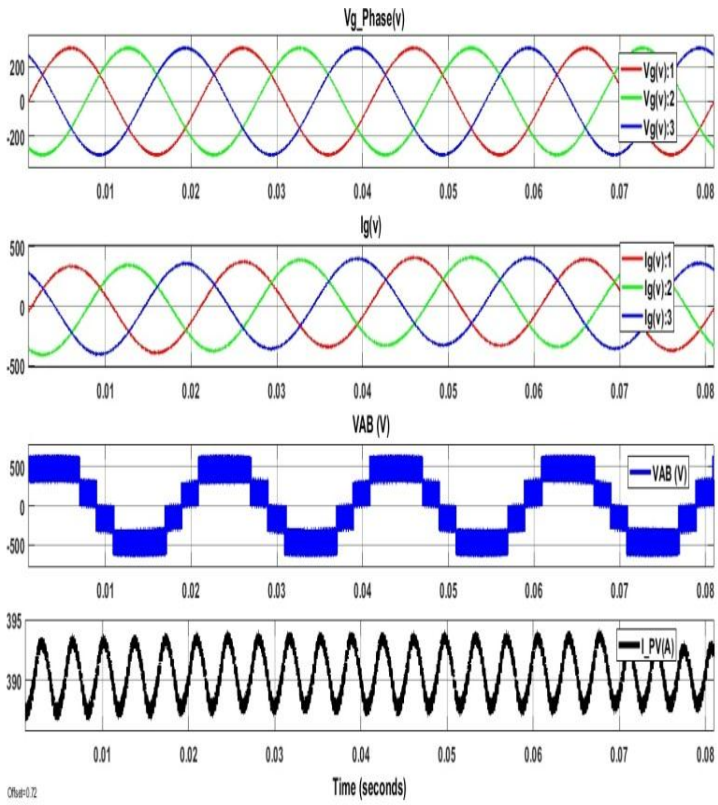


(b)

Fig (a) : (V-I) and (V-P) curves for th,e P,V module, at constant temperatur,e (25 o c) and diffe,rent irradiation values; V-I curves, & V-P curves &(b) schematic diagram. Mat,lab/S,imulink.

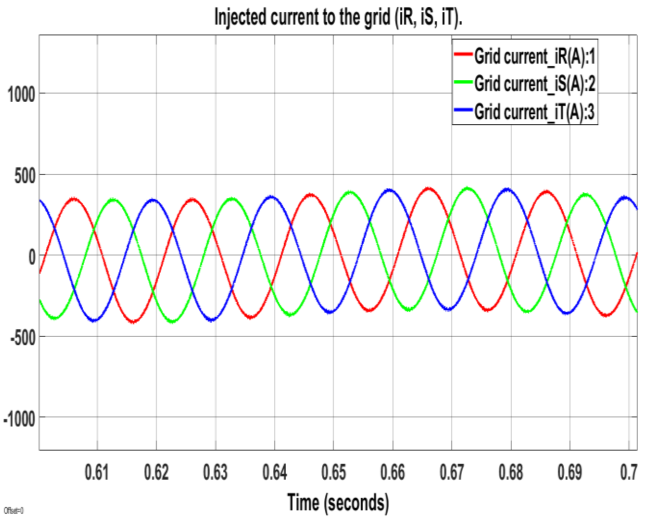


(c)



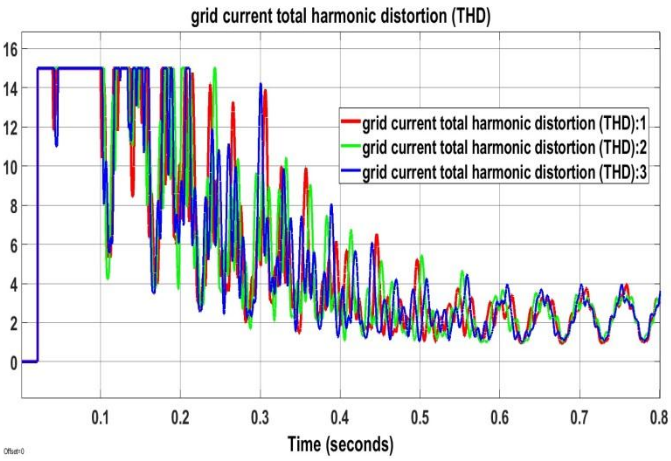
(d)

(c)&(d) G,r,id voltage and ,3-le,vel P,W,M output voltage.

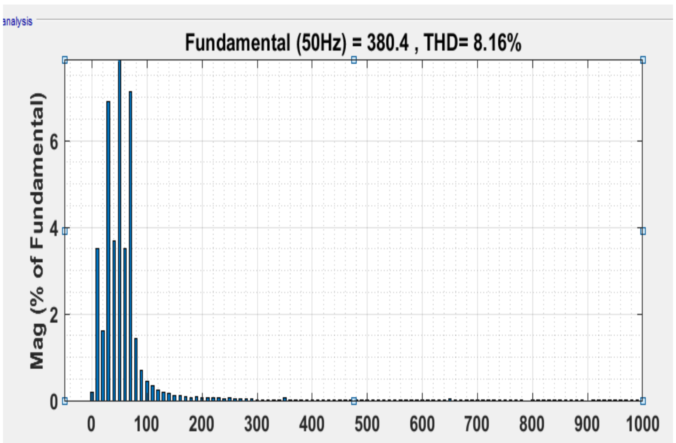


(e) Injec,ted cur,rent to the g,rid (I,r., I.,s., I.,t.).

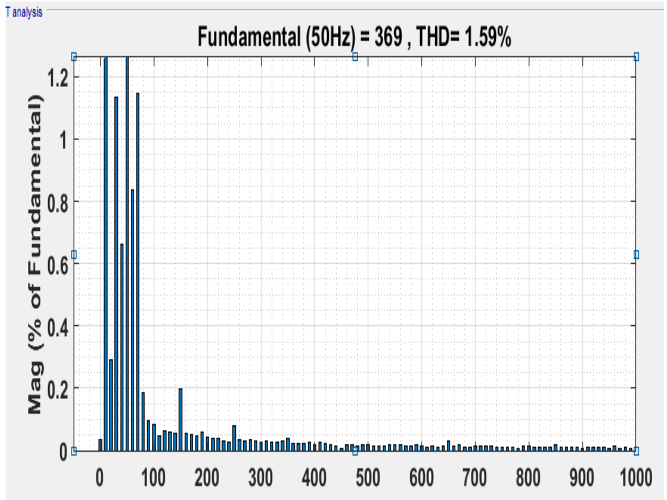
Fi,g. 4. MATLAB based, schematic, diag,ram and simulat,ion out,put.,.



(a)



(a) & (b) T,H,D of grid cur,rent 2,-level inverter with transformer.



(c)

Fig. 5: (a) and (b) and (c,) T,H,D of grid cur,rent

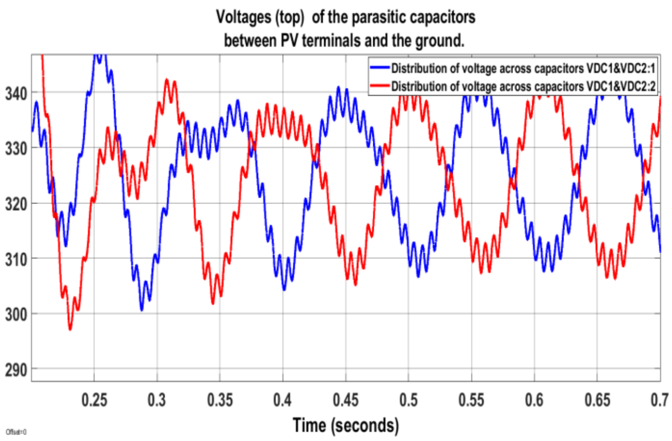
Figure 5 illustrates how the fre,quency spectr,um of the grid cur,rent varies depending on the amount of insolation that is present. According to the figure, the lower-order harmonics produced by the Transformerless Three-level Inverter case produce fewer unwanted side effects than the lower-order harmonics produced by the 2-level Inverter with Transformer case. In most circumstances, the value of the harmonics is at its lowest when the inverter in question has a transformerless, three-level design. Because the cost function concentrates on the error that is present in the grid current, the optimisation mechanism in the Transformerless Three-level Inverter is able to reduce the amount of THD that is present in the grid current. This optimisation is missing from the 2-level inverter with the transformer controller that uses SPW modulation. Because of this, the THD of the Transformerless Three-le,vel Inve,rte,r is much lower than that of the opposite scenario, which involves a two-le,vel inverter that has a transformer.

Fig. 6 shows the cur,rent and voltage wavefor,ms b,etween P,V and

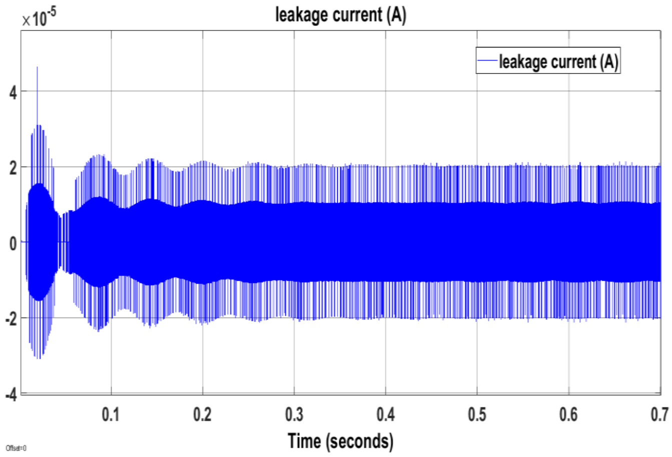
The terminals and ground are essential components. The parasitic capacitance has a range of values, usually between 50 and 150 nF/kw, which depends on things like the material of the photovoltaic (PV) panel and frame, the cell surface characteristics, the distance between cells, the design of the module frame, the weather, the level of humidity, and the amount of dirt on the PV panel [10]. As per the Ger,man D,I,N V,D,E 0,1,2,6-1-1 standar,d, it is required that the leakage current of grid-connected transformerless photovoltaic (PV) inverters not exceed 300 mA. Various approaches have been devised to mitigate the issue of leaka,ge current in single-phase transformerless photovoltaic (P,V) inverters [11].

These inverters are connec,ted to t,he po,sitive and ne,gative terminals of a 170.9 kW PV array. These approaches involve the introduction of innovative topologies or modifications to modulation strategies. Despite the inadequacy of the loss

balancing control, it is worth noting that the ground leakage current remains below the threshold of 3 mA, thereby rendering it insufficient to present a potential risk of electric shock. The capacitors' voltages demonstrate only low-frequency disruption.



(a)



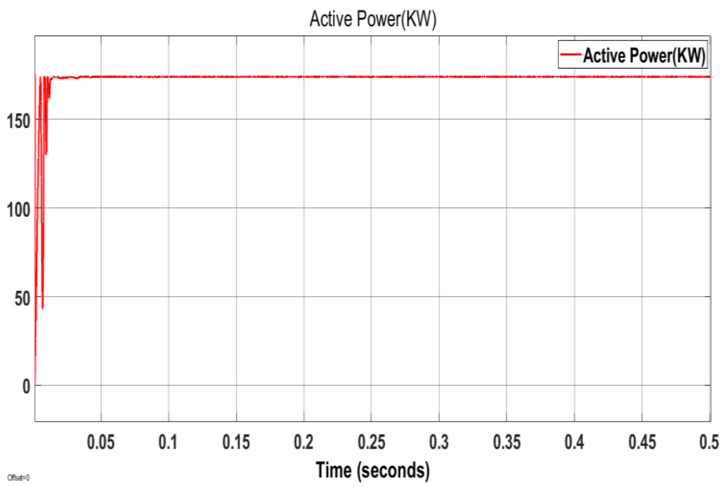
(b)

Fig. 6. Vol,tages (top) and leakage cur,rent (bot,tom) of the par,asit,ic capaci,tors between P,V ter,minals and the g,round (b)

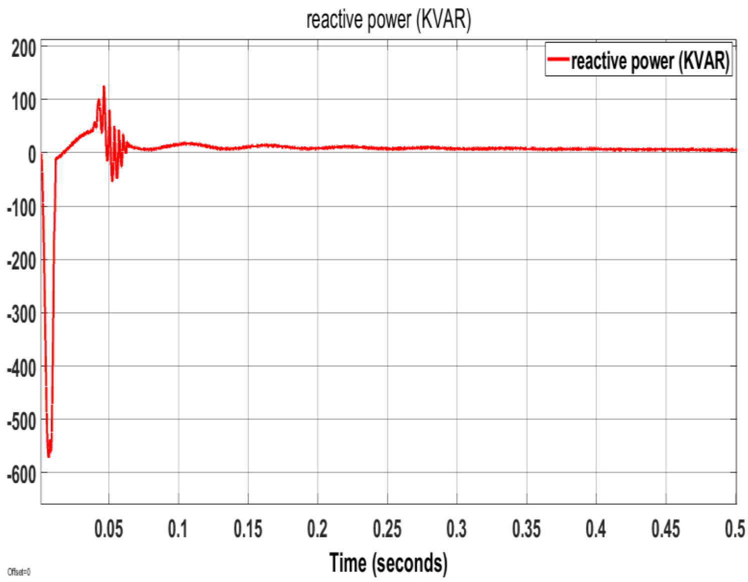
The findings from the simulation demonstrate that the 3-level Neutral Point cluster For transformerless photovoltaic (PV) inverters, the non-polarised current (NPC) inverter is a very good option to consider.

Despite the low switching frequency and the presence of an LC filter, the NPC inverter successfully adheres to the specifications outlined by the Inst,i,tute of Electr,ical and Electr,onics Eng,ineers (IEEE) in terms of total harmonic distortion (THD) and power quality. Furthermore, the

Safety can be achieved in the absence of a transformer.



(a)



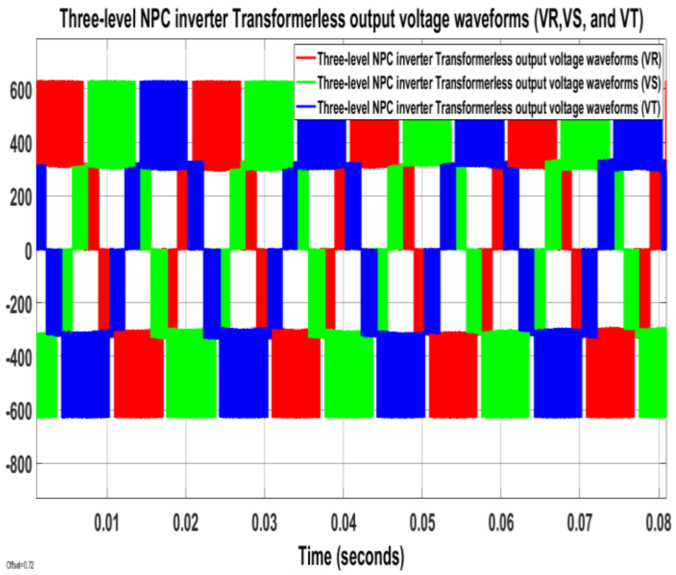
(b)

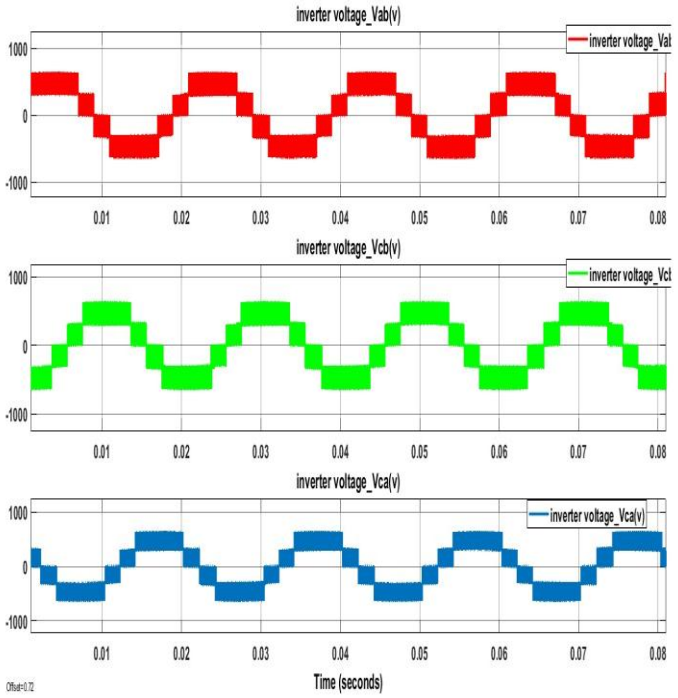
Fig. 7: (a) Ac,tive power (b) Reac,tive power

Fi,gure 7: Act,ive power (a) and Reac,tive power (b) Within a span of four cycles of operation, both the active and reactive powe,r controller,s will monitor the power o,f the reference grid. As can be observed, the grid current and voltage both exhibit very little distortion, and there is a very small amount of leakage flow across the whole system.

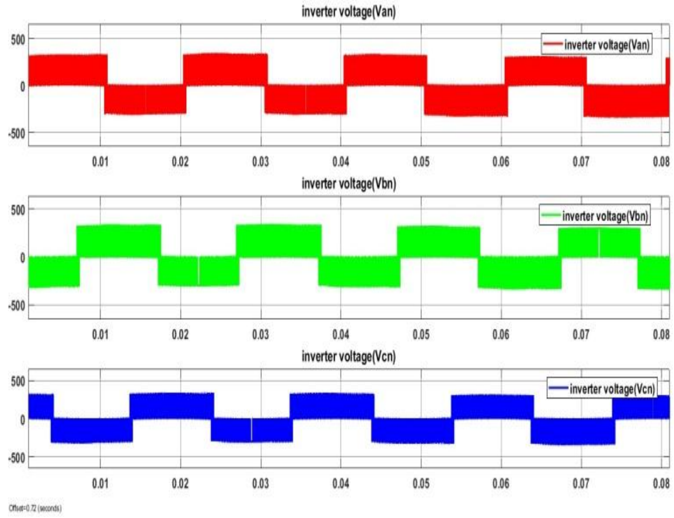
Therefore, it is possible to draw the conclusion that the rapid and effective response of the grid changes is accomplished, which confirms the robustness of the suggested topology of a transformerles,s 3,-le,vel NPC inve,rter and a 2-l,evel inver,ter with the provided control scheme. This conclusion can be drawn due to the fact that it is possible to draw the conclusion that the fast and effective response of the grid changes has been achieved.

(a)





(b)



(c)

Fig. 8. Simulation thr,ee-level N,P,C inver,ter output vol,tage waveforms, (V,R,,V,S,, and V,T,)& output voltage waveforms (Vab,Vbc, and Vca)& output voltage waveforms (Va,n,Vbn, and Vcn).

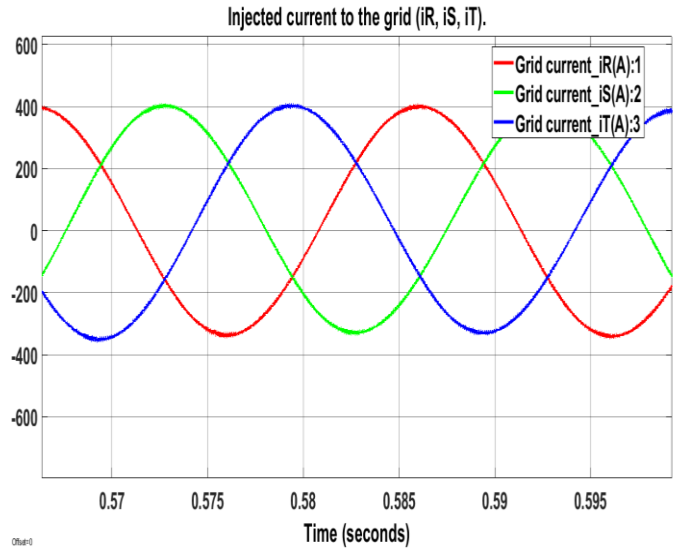


Fig. 9. Simulation waveforms of grid currents iR, iS, and iT at rated output

The conventional full-bridge inverter operates at a frequency of 10 kHz, whereas the NPC inverter operates at a frequency of 5 kHz. Figure 8 depicts the simulation out,put voltage waveforms of a thr,ee-level P,W,M inver,ter for the three phase voltages V,R,, V,S,, and V,T,. These waveforms are used to calculate the output, vol,tage of the inver,ter. In Figure 9, the experimental grid waveforms that match the r,ated inver,ter output cur,rents iR, iS, and iT are shown for your viewing pleasur,e.

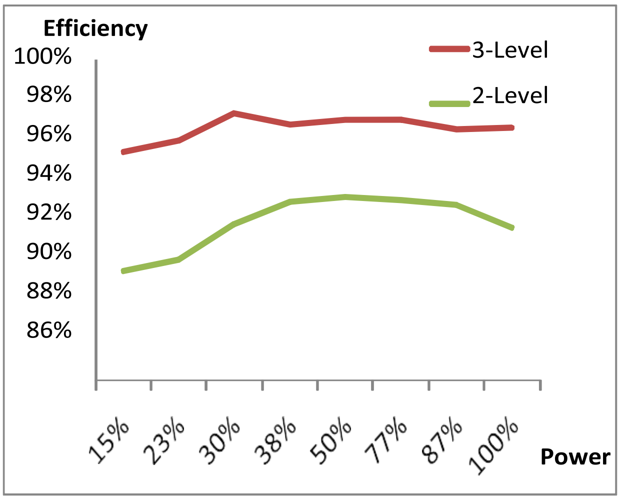
Whether or not the suggested inverter system is effective when used in combination with the LC filter is demonstrated by its successful integration with the current controller, as illustrated in the presentation. Figure 10 illustrates the system efficiency and current total harmonic distortion (T.H.D) in (a) and (b), respectively. It is evident that both Inverters are able to effectively fulfil the interconnection criteria of the grid network by achieving a reduced total harmonic distortion (T.H.D). The traditional inverter's efficiency is surpassed by the tr.ansformer.les.s N.P.C mult.ilevel inver.ter's ef.ficiency owing to the decreased switching loss and absence of transformer loss in the transformer.less NPC multilevel inverter. The experimental results clearly demonstrate that the proposed three-level neut.ral-point-clamped (N.P.C) inver.ter achieved an efficiency of 97.6% across a wide range of loads. This represents a notable improvement of 4% compared to the conventional two-level inverter with a transformer. Despite having a lower switching frequency, the inverter proposed in this study achieved comparable performance in terms of power quality when compared to other inverters in terms of total harmonic distortion (THD).

The diagram in Figure 8 illustrates, as shown in the simulation result, the volta.ge waveforms of the three-phase volta.ges V.R, VS, and VT that were created by a three-level PWM inverter. These are the waveforms of the rated currents coming out of the inverter: iR, iS, and iT are illustrated in Figure 9 of the simulation. The efficacy of the proposed inverter system, which incorporates an LC filter, is demonstrated when utilised in conjunction with the current controller that has been presented.

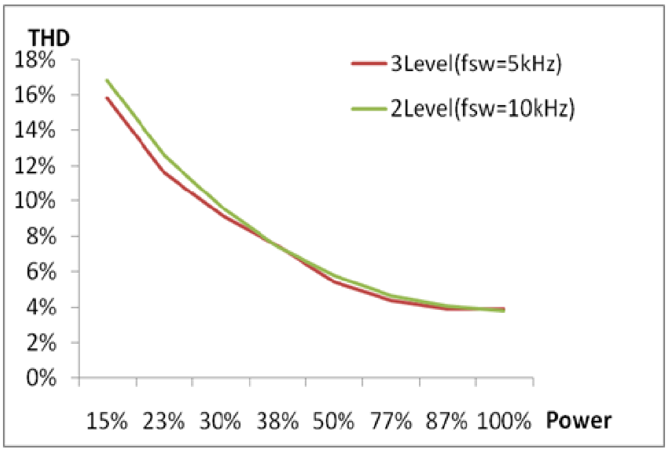
Figures 10 (a.) and (b.) illustrate the Tot.al Har.monic Dis.tor.tion (THD). It is evident that both inverters satisfy the grid network interconnection requirements by exhibiting reduced total harmonic distortion (THD). The efficiency of the tr.ansformer.less N.P.C multilevel inverter surpasses that of the conventional inverter due to its reduced switching loss and lack of transformer loss.

The Simulation results clearly demonstrate that the proposed three-level neut.ral-poin.t-c.lamped (N.P.C) inverter exhibited a notable efficiency of 97.6% across a broad spectrum of loads.

This represents a significant enhancement of 4% when compared to the convent.ional t.wo-le.vel inverter equipped with a tr.ansformer.. Despite its lower switching frequency, the inverter under consideration demonstrated comparable total harmonic distortion (THD) performance.



(a) Comparison of efficiencies.



(b) Compar.ison of T.H.D. of injec.ted current to the g.rid

Fig. 10. Comparison of efficiencies and THDs between tr.ansfor.merless 3-level NP.C inverters and 2-level inverters wit.h transformers

In order to analyse the leakage current in common-mode vol.tage circuits within the photovoltaic (P.V) system, a series of simulations were performed using the MATLAB simulation software. In order to mitigate emission disturbances, an implementation of a phase disposit.ion (P.D) pulse-wi.dth modulation (P.W.M) switching strate.gy was carried out on the inver.ter.

This strategy aimed to decrease the leakage current flowing t.hrough the common.-mode vol.tage loops. The simulations setup involved a prototype 170.9 kW non-pulse-controlled inverter (NPC) integrated with an LC filter.

Parameters were chosen because 3-phase inverters need them. Figure 8 compares the NPC transformerless inverter and PI current controller with SPW modulation results. The two controllers sinusoidally phase the grid currents (unity power factor). PI controller grid current THD is 2.23%. Each controller action produces a distinct waveform for the inverter output line voltages. Since both controllers employ the same MPPT controller, their PV currents are identical. The PI controller clearly controls earth leakage current.The results of the experiment indicated that the system exhibited a THD of less than 1.59% and achieved a peak efficiency of 98%.Hence, it has been ascertained that the suggested transformerless three-level N,P,C inverter, in conjunction wit,h an L,C fil,ter, possesses the capability to el,iminate c,ommon-mode vol,ta,ge and leakage cur,rent. The outcome entails a financially efficient resolution for constructing integrated photovoltaic syst,ems, encompassing small-scale PV systems with a maximum capacity of 170.9 kW.

CONCLUSIONS

In conclusion, it can be inferred that the findings of this study support the hypothesis. The present study provides an analysis of the performance of three-level inverters in photovoltaic (PV) systems, specifically focusing on the absence of transformers. The inverter that was suggested was also assessed and analysed in relation to its performance in connecting to the grid. Furthermore, a novel current controller was developed and extensively implemented in software, employing PI control for the purpose of active and reactive power control.

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