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# COMPARISON OF DUAL SOURCE TFET USING DIFFERENT DIELECTRIC MATERIALS

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**Abstract** - *The potential of high-k gate dielectric materials in improving the performance of FET. Dielectric material is used to increase the high conductance and reduces leakage. Using the different dielectric materials of $HfO_2$, $SiO_2$ and $Si_3N_4$ in dual source TFET are analyzed and compared to get the increased-ON current and decreased OFF current. High-k dielectric materials like hafnium dioxide ($HfO_2$) with dielectric constant in the range 22 to 25 give better performance than silicon dioxide and silicon nitride. The performance analysis of TFET with $HfO_2$, $SiO_2$, $Si_3N_4$ as gate dielectric is done using Silvaco-Atlas TCAD to understand the betterment of behavior of FET with high-k dielectric. FETs with high-k gate dielectric materials can be used in applications where power consumption and thermal stability are crucial[1].*

***Key Words*: *Dual source tunnel FET, Band to band tunneling, High-K dielectric material, High conductance***

## 1. INTRODUCTION

The exponential increase in number of transistors on an integrated circuit over time was first predicted by Moore's Law. Since the early 1970s, the metal oxide semiconductor-field-effect-transistor (MOSFET) has been recognized as the most promising device in VLSI circuits, because of its simpler structure, lower cost to fabricate and lower power consumption compared to bipolar and junction field– effect transistor (BJTs and JFETs). The demand for integrated circuits in the industry with greater functionality and lower cost performance requires an increase in chip density which demands scaling of the device. Scaling of silicon dioxide dielectric was once been viewed as an effective approach to enhance transistor performance in complementary-metal-oxide-semiconductor (CMOS). In past few decades, reduction of the thickness of gate dielectric below 2 nm, which is close to the physical limit, has led to huge increase in gate leakage current due to obvious tunnelling effect. On further scaling of the device, the leakage currents through Silicon dioxide ($SiO_2$), currently used dielectric, are intolerable due to high power consumption and low breakdown voltage. To continue the downward scaling, high-k dielectric materials are currently inconsideration for gate dielectric in MOSFET devices which play a major role in affecting threshold voltage ($V_t$). As the name suggest, these materials have high dielectric constant (high k) which improves the oxide capacitance, has low gate leakage current thus providing better stability to the device, lower power dissipation and higher breakdown voltage

### 1.1 PRINCIPLE

The TFET operation is based on band-to-band tunnelling (BTBT) method. BTBT process creates a tunnelling window through which the tunnelling of carriers from the valence band into the conduction band occurs. When the gate voltage is about to zero, the TFET is in the OFF state. The conduction band in the channel lies on top of the valence band in the source. As a result, BTBT is inhibited and therefore the TFET is in the OFF state with very low drain current. When the gate voltage is increased, the gate voltage modulates the carrier density below the gate and the conduction band in the channel is pushed down. Once sufficiently high voltage is applied to the gate, there's band bending at the source such the valence band in the source and therefore the conduction band within the channel get aligned. As a result, electrons in the valence band in the source will tunnel to the conduction band in the channel. The electrons that tunnel into the channel is swept to the drain terminal by the positive bias of the drain. This forms the premise of operation for an n-type TFET. It ought to be noted that, not like a MOSFET, a TFET is an ambipolar device. For example, an n-type TFET with the key contribution of electrons within the current transport will exhibit a p-type behavior with the major contribution of holes in the current transport, if a negative bias is applied to the gate.

### 1.2 DIELECTRIC MATERIALS

Dielectric materials are substances which are poor conductors of electricity. They are also called as insulators with an effective support of electrostatic fields. The flow of current is kept to a minimum when a dielectric is placed between opposite charged poles without interrupting the electrostatic. Important properties of a dielectric are its ability to support an electrostatic field while dissipating minimal energy in the form of heat, the extent to which a substance concentrates the electrostatic lines of flux. Substances with a low dielectric constant include a perfect vacuum, dry air, and most pure, dry gases such as helium and nitrogen. Materials with moderate dielectric constants include ceramics, distilled water, paper, mica, polyethylene, and glass. Metal oxides, in general, have high dielectric constants.

Dielectric materials with high dielectric constants can be used as gate dielectric in TFET. The dielectric material examined in this study in detail is hafnium oxide, silicon

dioxide and silicon nitride. High-k dielectric material gives high value of oxide capacitance ($C_{ox}$) which may influence the threshold voltage ($V_t$) and working of the device. The dielectric layers with higher electrical permittivity are used for thicker films to reduce the leakage current and improve the reliability of the gate dielectric layer with electrical thickness equal to ultra-thin $SiO_2$ layer. High-k dielectric materials are chosen with the properties of High Permittivity, Ability to reduce the leakage current, Lower power consumption, Lower direct tunnelling effect, Stable over silicon substrates.

## 2. PROPOSED MODELLING

The proposed system designs an optimal dual source tunnel FET structure using different dielectric materials of $HfO_2$, $SiO_2$, and $Si_3N_4$ are analyzed and compared to get increased ON current, reduce OFF current and improve $I_{ON}/I_{OFF}$ current ratio. FETs are the dominant transistors in digital circuits that form the basis of modern electronics. Over the globe we have high demand for efficient processors with high density chips. Scaling is the common process followed to achieve high packing density of FETs. Scaling of FET is limited with the decrease in thickness of common gate dielectric silicon dioxide ($SiO_2$). Silicon dioxide gate dielectric on scaling below 2nm results in tunnelling and high-power consumption, which in turn reduces the device reliability.

This work explores the potential of high-k gate dielectric materials in improving the performance of FET. Dielectric material is used to increase the high conductance and reduces leakage. Using the different dielectric materials of $HfO_2$, $SiO_2$ and $Si_3N_4$ in dual source TFET are analyzed and compared to get the increased-ON current and decreased OFF current.

High-k dielectric materials like hafnium- dioxide ($HfO_2$) with dielectric constant in the range 22 to 25 give better performance than silicon dioxide and silicon nitride. The performance analysis of TFET with $HfO_2$, $SiO_2$, $Si_3N_4$ as gate dielectric is done using Silvaco-Atlas TCAD to understand the betterment of behavior of FET with high-k dielectric. FETs with high-k gate dielectric materials can be used in applications where power consumption and thermal stability are crucial

## 3. RESULT AND DISCUSSION

**STRUCTURE FILE:**

The structure file provides the image of the device. This file reveals different materials used in various regions of the simulated device. The net doping concentration, electric field of the device can be analyzed using the structure file.

The following figures show the structure file of dual source:

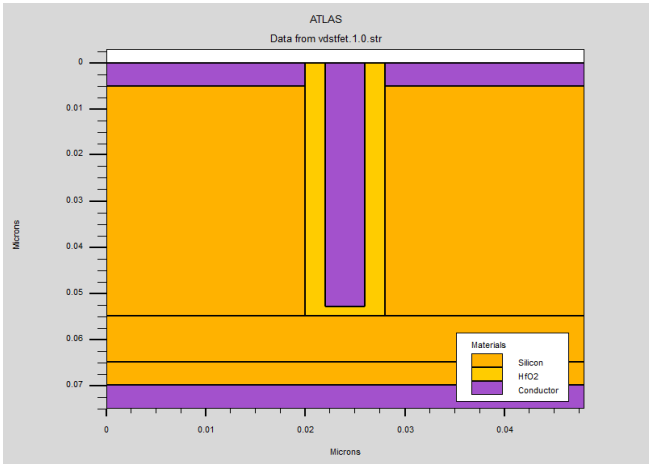


**Fig- 1** Structure of Dual source TFET using dielectric material Hafnium dioxide ($HfO_2$)

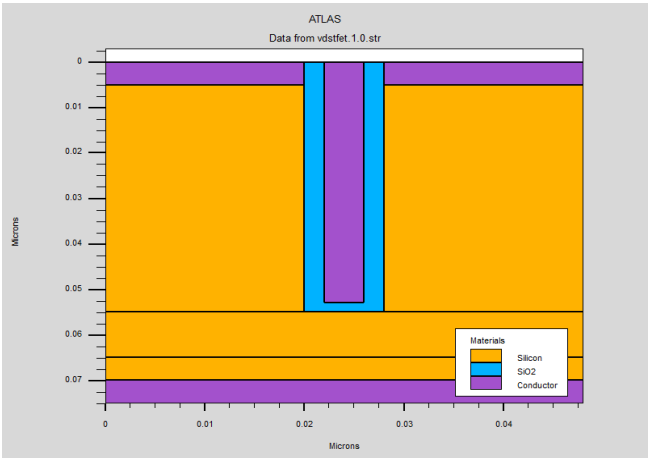


**Fig- 2** Structure of Dual source TFET using dielectric material silicon dioxide ($SiO_2$)

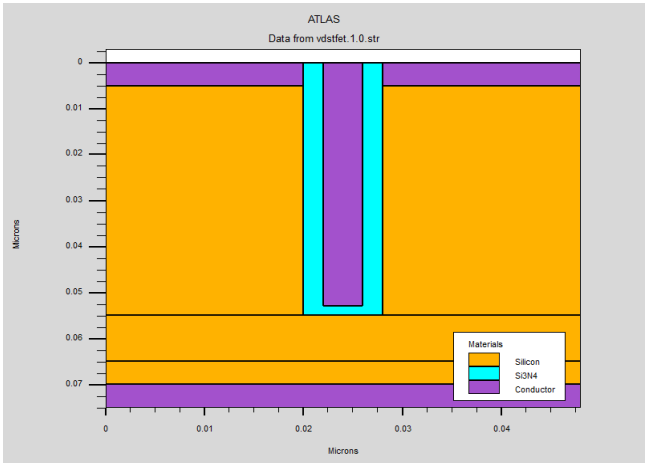


**Fig- 3** Structure of Dual source TFET using dielectric material silicon nitride ($Si_3N_4$)

The first source region of the device covers the minimum value of 0.000 and maximum value of 0.020 in x-axis and it covers the minimum of 0.005to 0.055 in y-axis and the second source region covers the minimum value of 0.028 and maximum value of 0.048 in x-axis and it covers the minimum of 0.005to 0.055 in y-axis. The channel region of the device covers the minimum value of 0.00 and maximum value of 0.050in x-axis and it covers the minimum of 0.055 to 0.065 in y-axis. The drain region of the device covers the minimum value of 0.000 and maximum value of 0.050 in x-axis and it covers the minimum of 0.065 to maximum of 0.070 in y-axis. The gate dielectric materials hafnium dioxide, silicon dioxide and silicon nitride cover the minimum of 0.020 to maximum of 0.028 in x-axis and minimum of 0.00 and maximum value of 0.052.

LOG FILE:

The log file represents the $I_D$-$V_{GS}$ characteristics of the simulated device.

- If the gate to source voltage $V_{GS}$ increases, then the drain current $I_D$ also increases. If the gate to source voltage $V_{GS}$ decreases, then the drain current $I_D$ also decreases. If the depletion width increases $V_{GS}$ decreases and if the depletion width decreases $V_{GS}$ increases.

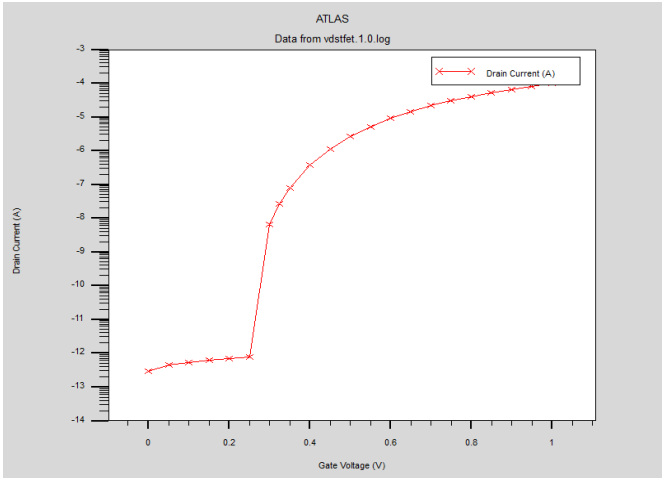


**Fig- 4** $I_D$-$V_{GS}$ Curve of dual source TFET using the dielectric material hafnium dioxide ($HfO_2$)

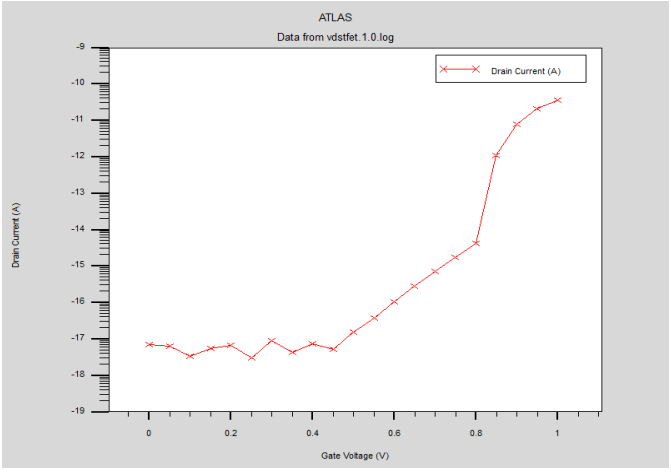


**Fig- 5** $I_D$-$V_{GS}$ Curve of dual source TFET using the dielectric material silicon dioxide ($SiO_2$)

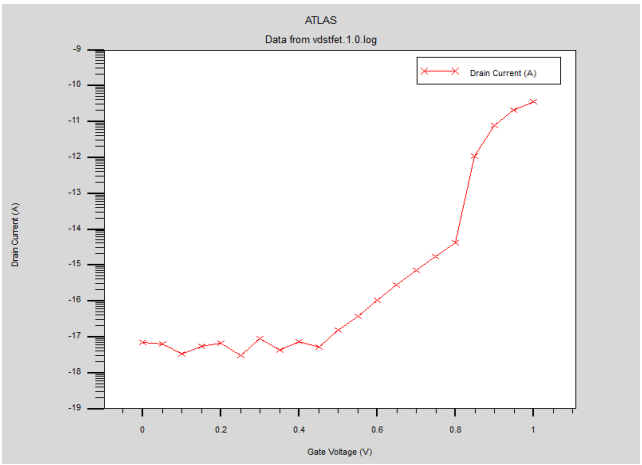


**Fig-6** $I_D$-$V_{GS}$ Curve of dual source TFET using the dielectric material silicon Nitride ($Si_3N_4$)

## 4. CONCLUSIONS

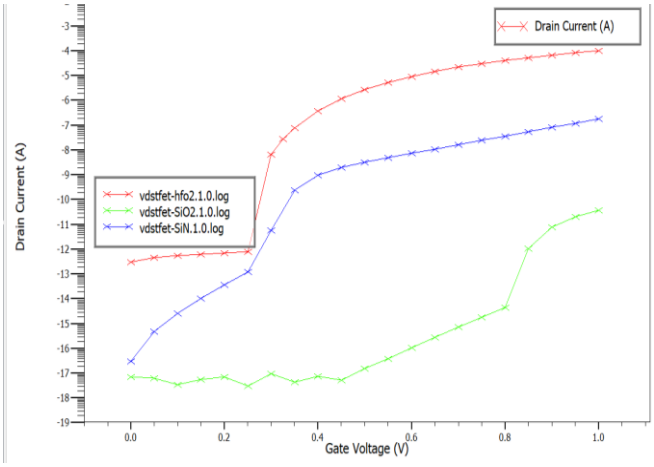


Fig- 7 Comparison of $I_D$-$V_{GS}$ Curve of dual source TFET using $HfO_2$, $SiO_2$ and $Si_3N_4$

This graph shows that hafnium dioxide provides high ON current and low OFF current are compared to the silicon dioxide and silicon nitride. Because of this characteristics hafnium dioxide reduces leakage current than silicon dioxide and silicon nitride. The implementation of high-k dielectrics in FETS is one of several strategies developed to allow further miniaturization. The leakage current of FETs with $HfO_2$ as gate dielectric is lower than the devices with same equivalent oxide thickness of $SiO_2$ and $Si_3N_4$. The ON current and OFF currents are the major considerations in the low leakage current structures explored in the work. Low K dielectrics material cause more leakage current while increased gate capacitance. High K dielectrics material allows increased gate capacitance without the associated leakage effects. It is concluded that due to the high dielectric constant, dielectric material hafnium dioxide produced the high ON current and reduces OFF current than the silicon dioxide and silicon nitride.

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