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Improved High Gain Dc-Dc Converter with Reduced Noise

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Abstract - *When it comes to sustainable energy, solar photovoltaic energy production is crucial. The photovoltaic cells use a portion of the sun's energy, which is copious and readily available. Therefore, the energy conversion mechanism should have great efficiency. Consequently, a high-efficiency dc-dc converter for low-voltage solar sources is suggested. Great voltage gain and high efficiency are used by the suggested converter to increase DC voltage. Dual active clamping circuits and a resonant voltage doubler rectifier are used in the proposed converter. Power switches experience less voltage stress on the low voltage side. Output diodes can be turned off with zero current on the high-voltage side.*

Key Words: *Photo - voltaic (PV), power efficiency DC-DC converter.*

1. INTRODUCTION

The primary technology for future solar-powered electricity production is the photovoltaic (PV) module-integrated converter (MIC) system [4], [5]. There is a unique power conversion system for every PV module. The PV module's maximum power is produced via the power conversion system [7]. A high-efficiency and inexpensive power conversion scheme needs to be created in order for the PV MIC system to be economically viable. The PV module often exhibits a low-voltage characteristic [15]. Low voltage (the dc voltage of a PV module) must be converted into high voltage in order to supply electricity to the grid [14]. A high-voltage gain dc-dc converter is therefore required.

The integrated cascade boost converter's switch voltage stress is equal to high voltage, and the current stress is significant [1]. Conduction losses go up and the converter's efficiency goes down with a cascade boost converter. By increasing the coupled inductor's turns ratio, a converter with a coupled inductor can simply increase its voltage gain. It does, however, have a sizable steady-state inductance. The overall efficiency is decreased as a result of the large steady state inductance's increased losses [12]. The converter layout is also intricate, and the design process is as difficult. The magnetic components, such as the inductor or the transformer, won't be needed for the SC converters. Thus, a high amount of switching frequency can be achieved. However, in order to obtain high-voltage gain, more power components are needed, which raises the converter's complexity and price [6].

Due to their components inability to withstand high power circumstances, the majority of single-phase isolated DC/DC converters appear inadequate and deficient. The losses of the converter rise as the phase shift does in a multiphase dual active bridge converter. Additionally, the design uses two switch legs, which means that a three-phase converter needs 12 power switches, increasing the number of switches, switching losses, and converter price [10]. Due to its high leakage inductance (0 D 0.333), the Multiphase ZVS PWM DC/DC Converter has a limited duty cycle and experiences high circulating energy in the main side during free-wheeling periods [3].

Photovoltaic sources have made use of the active-bridge dc-dc converter [9], [2]. At zero voltage, the power switches on the low-voltage side are activated. However, due to its reverse-recovery current, the output diode on the high-voltage side suffers from significant switching power losses. To lessen switching power losses at the high voltage side, the half-bridge dc-dc converter has been introduced [16]. By using a voltage doubler rectifier circuit, the output diodes are turned off at zero current. However, this requires a second half-wave rectifier, which raises switching power losses. As an alternative, low-voltage PV sources have been employed with active-clamped dc-dc converters [8], [13]. It makes use of the resonant voltage doubler rectifier and active-clamping circuits.

For low-voltage PV sources, a high-efficiency dc-dc converter is suggested in this research. By utilising a dual active-clamping circuit, an active-clamped dc-dc converter is provided. On the low-voltage side, the voltage stress on power switches is lessened. The suggested converter's operation is described. The PSIM programme is used to confirm the proposed converter's performance. The simulation results demonstrate that at 41-V voltage source for 330-W output power, a high efficiency of 98 percent is attained.

2. PROPOSED DC-DC CONVERTER

2.1. Converter Description

Fig. 1 depicts the proposed DC/DC converter with a voltage doubler rectifier and dual active clamping circuits. The DC/DC converter that is being suggested is an AC link chopper. Dual active clamping circuits were used to make the inverter part. The rectifier part employs a resonant voltage doubler rectifier. The dual active-clamping circuit (S_2, S_3, C_c), transformer T, and resonant voltage doubler rectifier are the major switches (S_1, S_4) in the proposed DC/DC converter (L_{lk} , C_r , D_{o1} , D_{o2}). With little dead time, the primary switches (S_1, S_4) and auxiliary switches (S_2, S_3) are designed to work in tandem.

Metal-oxide semiconductor field-effect transistors are used in each switch. Except for their output capacitors C_{S1}– C_{S4} and body diodes D_{S1}– D_{S4}, they are regarded as ideal switches. The input capacitor's name is C_i. The clamping capacitor is C_c. The output capacitor is named C_o. Thevoltages V_i, V_c, and V_o of the capacitors C_i, C_c and C_o are each large enough to be regarded as constants. The transformer has a leaking inductor L_{lk} and a magnetising inductor L_m. L_{lk} is thought to be somewhat smaller than L_m. The transformer has a turns ratio of 1:N, where N=Ns /Np. The resonant capacitor is called C_r.

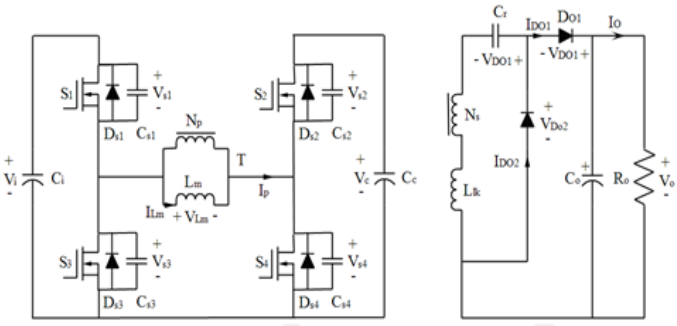

Fig. 1: shows the proposed DC-DC converter's circuit diagram.

2.2. Converter Operation

The suggested DC-DC converter's switching waveforms are shown in Fig. 2 for one switching period T_s =($1/f_s$). Figure displays the switching waveforms at the primary side (a). The switching waveforms at the secondary side are depicted. Six switching modes are available in the proposed DC/DC converter during T_s. The main switches' on-time provides the basis for the duty ratio D. S_2 and S_3 have been deactivated prior to t = t_0. When the principal current ip travels through the body diodes D_{S1} and D_{S4}, the voltages V_{S1} and V_{S4} have been zero.

The time interval during this mode is regarded as minimal in comparison to T_s because the switch output capacitor C_S (= C_{S1}= C_{S2}=C_{S3}=C_{S4}) is so small. S_1 and S_4 are turned ON once more to start the next switching cycle.

2.3. clamping capacitor voltage varies with duty cycle.

The inductor volt-second balancing principle states that the average value, or dc component, of voltage supplied across an ideal inductor winding must be zero. This idea also holds true for every transformer winding and other magnetic devices with numerous windings.

The voltages V_c and V_r are expressed as a result of the voltage-second balance relation on the magnetising inductor L_m.

$$V_c = [D/(1-D)]\, V_i$$

$$V_r = (1-D)\, V_o$$

The output voltage V_o and the input voltage V_i are obtained using the voltage-second balance relation on the secondary winding of T during T_s.

$$V_o/\, V_i = N/(1-D)$$

The input voltage V_i regulates the maximum voltage stress of S_1 and S_3. The clamping capacitor voltage V_c is the maximum voltage stress that S_2 and S_4 can withstand. Figure 4 depicts the relationship between the duty ratio D and the clamping capacitor voltage V_c. The inverter portion of the suggested DC/DC converter employs a dual active-clamping circuit. When using a dual active-clamping circuit, the clamping capacitor voltage is always lower than when using a traditional active-clamping circuit.

By adopting the traditional active-clamping circuit, it means that the switch voltage stress of the proposed DC/DC converter is consistently lower than the switch voltage stress of the previous converter [12].

The clamping capacitor voltage V_c may be lower than the input voltage V_i, particularly when the duty cycle ratio is less than 0.5. It is especially helpful in low-voltage PV systems where switching power losses account for more than half of the total power losses.

D. Conditions for turning off zero current

Before turning ON the output diodes D_{o1} and D_{o2}, the currents via the output diodes i_{Do1} and i_{Do2} should be zero. Before the output diode is turned OFF, the series resonance in Mode 1 and Mode 4 should have completed its half-resonant time. For the output diodes to be turned off at zero current, the following requirements must be met.

$\text{Sin}\,[\omega_c D_{max} T_S] = 0$ if $D_{max} \leq 0.5$

$\text{Sin}\,[\omega_c (1-D_{max}) T_S] = 0$ if $D_{max} > 0.5$

The resonant frequency,

f_r, should be greater than the critical resonant frequency, f_c, to enable zero-current turnoff of the output diode.

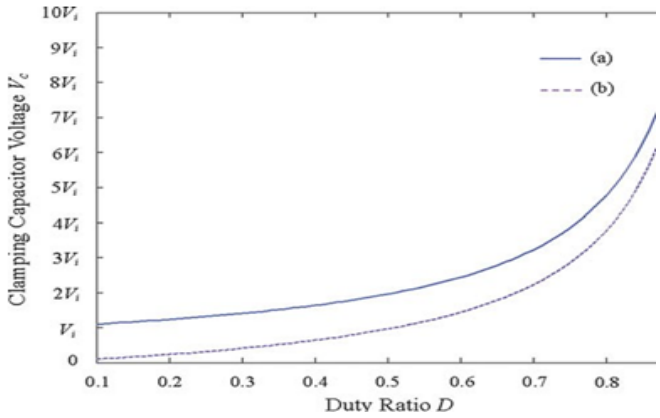

Fig. 2: shows the relationship between the clamping capacitor voltage Vc and the duty ratio D: (a) in the scenario of the traditional active-clamping circuit, and (b) in the scenario of the dual active-clamping circuit.

3. SIMULATION RESULTS

The simulation results are given using PSIM 9.0 software to support the theoretical study of the suggested topology.

Table -1: Simulation Parameters

Parameters	Value
Input voltage, V_i	40 V
Output voltage, V_o	409 V
Output power, P_o	330 W
Switching frequency, f_s	5 kHz
Input capacitor, C_i	13.2 nF
Clamping capacitor, C_C	680 µF
Switch output capacitor, C_S	500 pF
Transformer turns ratio, N	5
Magnetizing inductor, L_m	9 µh
Leakage inductor, L_{lk}	3 µH
Resonant capacitor, C_r	0.4 µF
Output capacitor, C_o	50 µF

Table - 1 lists the specifications of the various parts that make up the suggested DC/DC converter. A triangle and DC signal is compared in order to apply the gating signals to the gate terminal of the power switches. We may obtain equal-distance PWM pulses by comparing these two signals, and these pulses are then applied to the gate terminals of the power switches S1 to S4. Figure 6 displays the voltage across the switches. The input and output voltage simulation waveforms are displayed in Fig. 6. 41 volts is the typical input voltage. 409V is the average output voltage as measured. The input and output power waveforms are displayed in Fig. 6. About 337W is the input power. A 330W average output power has been determined. The difference between the input and output powers is minimal. Thus, the suggested DC-DC converter achieves high voltage gain and efficiency of 97.9%.

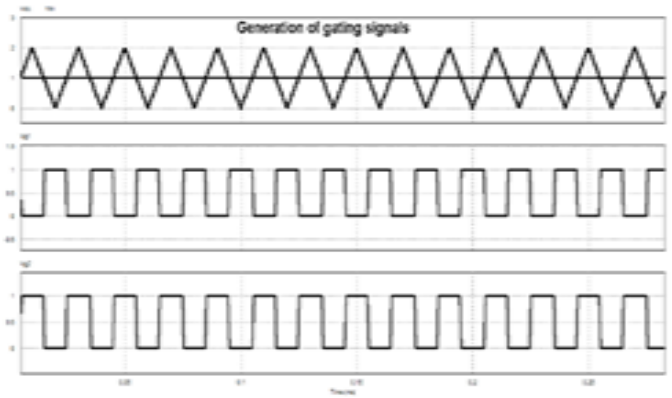

Fig. 3: shows the waveforms of the gate voltage (V_{g1} & V_{g2}), the DC signal (V_{dc}), and the carrier voltage (V_{tri})

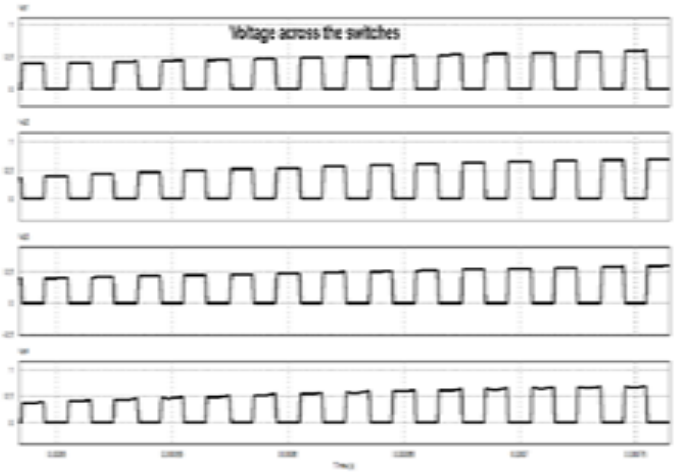

Fig. 4: Voltage waveforms over switches (V_{s1},V_{s2}, V_{s3} & V_{s4})

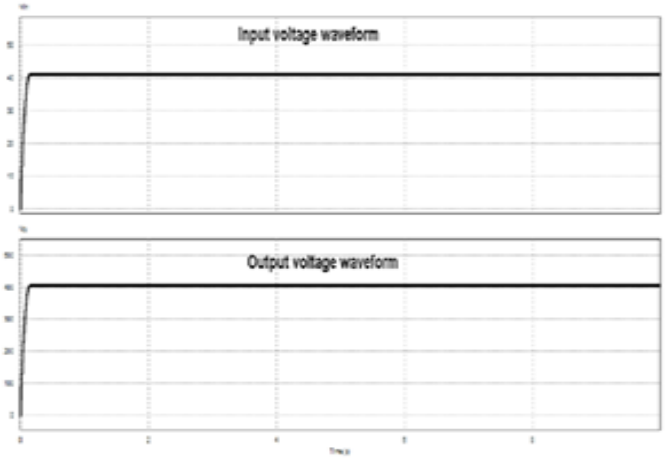

Fig. 5: Waveforms of input and output voltage (V_{in}, V_o)

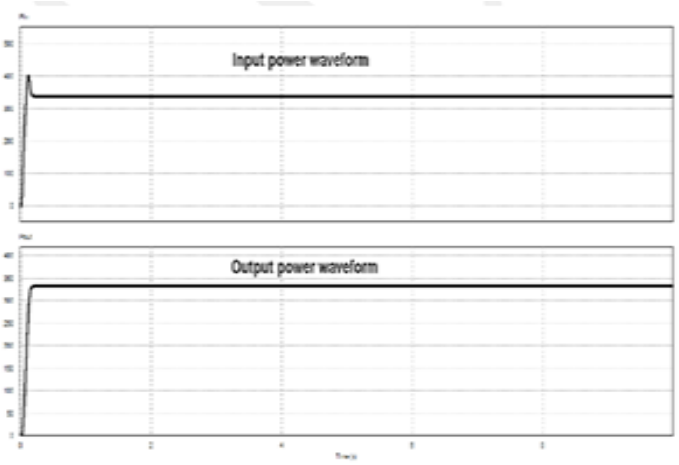

Fig. 6: Waveforms of input and output power (P_{in}, P_o)

4. CONCLUSION

A high-efficiency and high-gain DC/DC converter has been suggested for low-voltage PV sources as a way to provide efficient PV conversion. The proposed DC/DC converter's operation has been explained. Along with the circuit operating modes and accompanying key waveforms, the converter's synthesis was explained. The suggested converter improves power efficiency by decreasing switching power losses. High voltage conversion ratio and zero current output diode turn-off are provided by the suggested DC/DC converter topology.

PSIM is used to verify the proposed DC/DC converter. At 41-V input voltage and 340-Watt output power, the suggested converter achieves a high efficiency of 98 percent. The installation of a modified PI controller for output voltage regulation opens up the possibility of further efficiency gains. This can also enhance the dynamic and transient response. Future DC/DC converter prototypes could be produced with high gain and great efficiency.

REFERENCES

[1] B. Liu, S. Duan, and T. Cai, "Photovoltaic DC- building-module-based BIPV system: Concept and design considerations," IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1418–1429, May2011.

[2] C. Rodriguez and G. A. J. Amaratunga, "Long- lifetime power inverter for photovoltaic AC modules," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2593–2601, Jul. 2008.

[3] D. de Souza Oliveira, Jr. and I. Barbi, "A three- phase ZVS PWM DC/DC converter with asymmetrical duty cycle for high power applications," IEEE Transactions on Power Electronics, vol. 20, pp. 370-377, 2005.

[4] E. Serban and H. Serban, "A control strategy for a distributed power generation microgrid application with voltage- and current- controlled source converter," IEEE Trans. Power Electron., vol. 25, no. 12, pp. 2981– 2992, Dec. 2010.

[5] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," IEEE Trans. Power Electron., vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[6] K. K. Law, K. W. E. Cheng, and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," IEEE Transactions on Circuits and Systems I: Regula Papers, vol. 52, pp. 943-948, 2005.

[7] L. Zhang, K. Sun,Y. Xing, L. Feng, andH.Ge, "A modular grid-connected photovoltaic generationsystem based on DC bus," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 523–531, Feb. 2011.

[8] M. Barai, S. Sengupta, and J. Biswas, "Digital controller for DVS-enabled dc–dc converter," IEEE Trans. Power Electron., vol. 25, no. 3, pp. 557– 573, Mar. 2010.

[9] M. Cacciato, A. Consoli, R. Attanasio, and F. Gennaro, "Soft-switching converter with HF transformer for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 5, pp. 1678–1686, May 2010.

[10] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power

applications," IEEE Transactions on Industry Applications, vol. 27, pp. 63-73, 1991.

[11] Woo-Young Choi, "High efficiency dc–dc converter with fast dynamic response for low PV voltage sources," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 706-716, Feb. 2013.

[12] W. Tsai-Fu, L. Yu-Sheng, H. Jin-Chyuan, and C. Yaow-Ming, "Boost Converter With Coupled Inductors and Buck-Boost Type of Active Clamp," IEEE Transactiocns on Industrial Electronics, vol. 55, pp. 154-162, 2008.

[13] W. Y. Choi, J. S. Yoo, and J. Y. Choi, "High efficiency dc–dc converter with high step-up gain for low PV voltage sources," in Proc. IEEE ECCE Asia, Jeju, Korea, May 30/Jun. 3, 2011,pp. 1161–1163.

[14] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non isolated AC-module applications," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1253–1260, Apr.2011.

[15] Y. Fang and X. Ma, "A novel PV microinverter with coupled inductors and double-boost topology," IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3139–3147, Dec. 2010.

[16] Z. Liang, R. Guo, J. Li, and A. Q. Huang, "A high-efficiency PV module integrated DC/DC converter for PV energy harvest in FREEDM systems," IEEE Trans. Power Electron., vol. 26, no. 3, pp. 897–909, Mar. 2011.