EFFICIENT CURRENT MODE ADC: A REVIEW

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Abstract: - *The signals which are present naturally in our environment are analog in nature and they are very complicated when comes to their studies. Thus, to reduce the complications the analog signals which are present in the environment has to be converted into digital signals because these digital signals are much easier to study and to do research on them. Thus, for the process of conversion of analog to digital signals there is a device used known as analog to digital converter (ADC). Thus, the main concern is on the converters to make them more efficient and precise. In this paper, an algorithm is used to make the analog to digital converter more efficient when these are in there current mode. As, we have always worked in the voltage mode when it comes to the signal conversion from analog to digital. But, in this paper we have worked in the current mode rather than voltage mode. There are different algorithms present to convert signals from analog to digital while working in current mode but the algorithm ADC is the most beneficial conversion algorithm till date and it gives more precise and accurate output than other algorithms. Thus, in this paper algorithm ADC has been used to make the ADC more efficient while working in current mode.*

Key Words: Analog to Digital (ADC), Converter, algorithmic ADC, Characters of ADC, Flash ADC

1. INTRODUCTION

The most naturally occurring signals are analog in nature and these quantities are continues function in time. Most of the transducers also give analog output and hence the analog signals are of much importance. With the advent of digital computers an introduction to digital signals came into action. Computers can understand only digital data in the form of 0's and 1's.

When system engineers made their first attempt to input analog signal into digital computers at applying computational powers, speed and data handling capability, it became a challenge. Making digital computers to work with analog signals was more like working against the nature and hence it became time and energy consuming.

In 1965, analog devices has been found to have leadership roles in scheming and manufacturing devices that meets the requirements of the current markets for this an accurate relationship between tangible physics and abstract digit has been there.

Technology hasn't stopped evolving since ages and assures to move with an increasing pace with every increasing year. From large rooms sized computers to a handy smart phone processing tones of information in a fraction of second, from analog to digital, technology hasn't yet taken up a step back around us.

In earlier times when ideas travelled along with the people, taking years and years to collect knowledge and resources in order to foster the ideas into implementation, and a lifetime to accomplish it. Digital circuits brought a boon in field of technology, ideas now travel faster than people could actually moves and the world is revolving on the clock of seconds and information is everywhere. Our life is changing every moment and we are connected to this whole world with a click.

Now, machines and humans can actually communicate, circuits are achieving nanometer sizes and are a part of our daily lives. Smart devices are an indispensible part of our routine and they are actually performing everything we just think and desire.

All these advancement have been due to the digital conversions possible by using ADC conversion devices. ADC is basically analog to digital converters these converters convert the naturally occurring real world analog signals into digital signals used for computational purposes. On the basis of various parameters like fast speed, less resolution ADC's are used in digital high speed wire lines and communications which are wireless, oscilloscopes and radars. There are various types of ADC architectures out of which we have used algorithmic ADC. Due to its serial mode of nature, the operation of speed is high however less than flash which has a medium profile resolution. Another analog to digital converter architecture is successive approximation resolution worthy for low power and medium to high resolution having moderate rate of speed. Other architecture is sigma-delta ADC appropriate for low speed application and high resolution. Last and fastest architecture available is the flash ADC. It can be made operational at very fast rate due to the parallel operation but low resolution. Studies reveal that amongst all the existing converters, the algorithmic ADC provides the pros of the circuit functioning in terms of speed, less power and lower chip area. The algorithmic ADC is the best option for high speed low resolution applications.

In section 2 the conversion of analog signal into digital signal is shown. In section 3 types of ADCs are shown. In section 4 various characters of analog to digital converters are illustrated with some examples. In section 5 algorithmic ADC is described with its block diagram. In section 6 simulation result of ADC is proposed while it is working in low values of current as well as the high values of current.

2. CONVERSION FROM ANALOG TO DIGITAL SIGNALS

Sensing devices are a boon in today's technology, from being a simple thermometer to Electro-Mechanical industry. Various sensing devices are being made using microelectronics. A special branch knows as MEMS is working towards the development of these devices. Interfacing digital circuits with the sensor devices becomes simpler if the sensor devices are of digital nature. Due to the on/off nature of digital signals, various electrical components like switches, relays, & digital encoders are interfaced with easiness along with the gate circuits. It is requisite to electronically interpret analog signals into digital capacities, since when the devices of analog nature are intricate, interfacing becomes a complexity. The vice versa conversion of analog to digital is equally needed in a circuit implementing an ADC. [1] An Analog to Digital Converter takes analog electrical signal for example voltage or current as input and produces a binary digit output. A Digital to Analog Converter, on the contrary, takes an input of binary digit and gives an analog current or voltage as output. Most of the times used together in digital control systems to offer whole interface with analog sensors and output devices for control systems for example those used in automotive engine controls. For example, A-to-D conversion in radio frequency receivers, implant exceptional demands on the converter, and a style in receiver proposal have been to move the digitization nearer to the receiving antenna.

2.1. Process of Conversion from Analog to Digital Signals

The process of translating various naturally happening signals like pressure, temperature, voltage, current, distance, or light magnitude into a digital representation of that signal is carried out by Analog-to-Digital converters (ADC). [2]

Talking of data processing devices, wherein the input has to be analog and for interfacing it with computers for reading, understanding and manipulating the data, we need digital signals. Hence to convert the signals from analog to the digital an ADC is required for such processing devices.

Primary cause that digital signals are preferred over analog signals is that these signals proliferate more effectively than analog signals, broadly because digital impulses are properly-defined and structured, are simpler for electronic circuits to differentiate from noise, which is haywire.

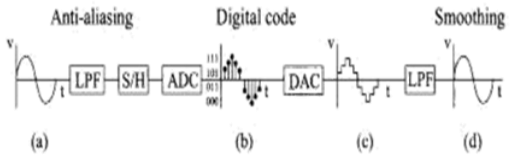


Fig-1: Conversion process by A-to-D and D-to-A

The basic principle of conversion of analog signal into digital signal is:-

The basic operation of analog to digital conversion and vice versa is shown in Fig.1, firstly the original signal (a) is analog in nature and is strained by an anti-aliasing filter also called LPF, used to suppress high frequency signals which might cause a consequence known as aliasing. Then the signal is sampled (if it is a voltage mode, in case of current mode this step can be skipped) and held for a given time interval and then using an ADC is converted into a digital signal (b).Further step is to convert the digital signal obtained, using a DAC that transforms the digital signal into an analog signal again (c). It is observed that the DAC has the output which is not as "even" as the signal given which are original in nature. Hence a low-pass filter is needed to return the analog signal back to its authentic form (also adding up the phase shift introduced during the process of conversions), banishing all the higher order signal components produced by the transformation. The above conversion process shows that an analog signal in (a) is a continuous and infinite valued in time signal whereas the digital signal in (b) is discrete with respect to time and quantized[2]. In simple words a signal having a continuous set of values for the entire length of time is called as continuous time signal. By the term values which are infinite, we infer that any value can be given to the signal among the defined factors of the system. For instance, if the peak magnitude that is the highest value of the magnitude of the sine wave is +1V, then the analog signal can be any value between -1 and 1 V (such as 0.253687852 V).

The digital signal, on the other hand, unlike analog are discrete in nature. By discrete we mean the amplitude varies by defined level by level with respect to time. It concludes that the digital signal is described for only individual frames of time.

3. TYPES OF ADC

While designing of ultra-low-power circuits, one has to remember the energy considerations point which drives the procedure from decision of architecture to real circuit implementation. Selecting architecture is a crucial point in the designing of such systems. An appropriate decision of architecture results in energy savings with respect to other parameters. On the other hand, a poor architectural choice can bring out an imperfect design despite how well the specific device parts are implemented. Though consumption of energy is primary in this but several other factors also gets affected by the choice of ADC architecture. ADC architecture can vary roughly by their achievable resolution, Propagation delay, and speed and power consumption. Fig.2 groups various ADC's according to its characteristics. Since low-area and high speed is the primary concern in the paper, Fig.2 shows that much architecture is poor choices. After evaluation we found that algorithmic ADC satisfies our constraint and hence we have preferred this over others. ADC's such as Time included require various sets of analog hardware, hence results in high power eating but very fast sampling rates. On the other hand, Folding and/or interpolation the number of comparators required gets reduced due to its recurring property, yet the architecture

are still not appropriate for low-power applications. Flash converters [3] are those which utilize for a given resolution a large range of comparators create the impractical in most applications requiring quite eight bits of resolution. Multi-step ADC additionally needs a comparatively great amount of analog hardware, due to which there is excessive power consumption in networks in which these have their applications. A number of the opposite distinguished ADC architectures, like Delta-Sigma, [4] ordered Estimate, group action and recursive, are rumored to figure with power consumption which is low.

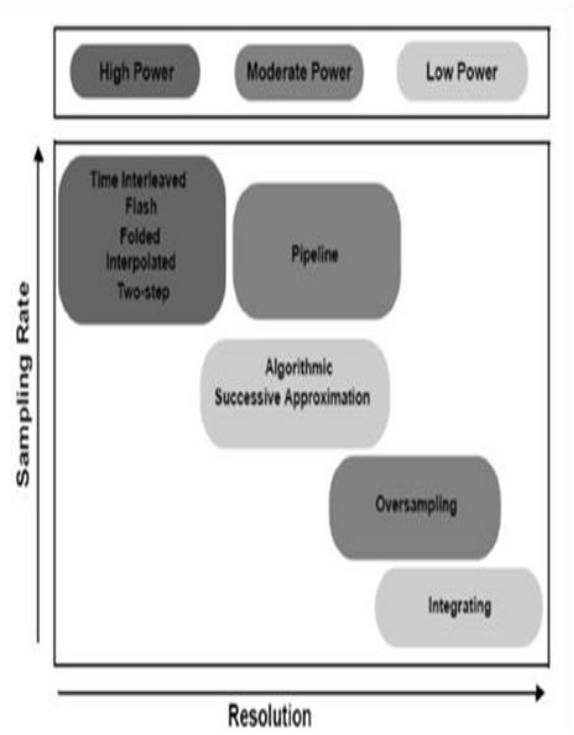


Fig-2: Analog to Digital Converter structures characterized by resolution, sampling rate and power consumption [5]

4. ADC CHARACTERIZATIONS

When an analog input signal is given to an ADC (be it a voltage or current), its function is to convert it into digital bits, while doing this it has to perform Quantization [1]

During the process, it has to "quantize" the enormous-valued analog signal converted into several sections due to which

Number of quantization levels = 2N…….. eq. 1

Where N represents the no of bits of an N-bit ADC

Let us consider the fig.3, given below and say it is a 3-bit ADC giving 3 digital output bits for an analog input signal VIN. We have plotted a graph between digital output code vs V_{IN}/V_{REF} and this plot can be extended for current modes as well.

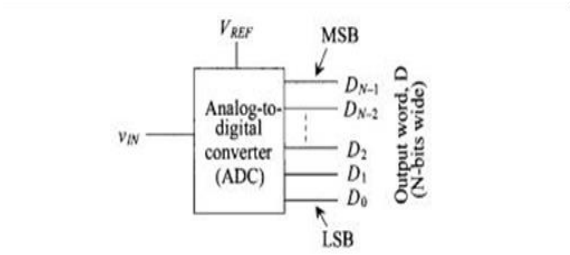


Fig-3: ADC Block Diagram

The ideal transfer curve of the ADC bears the resemblance to that of a staircase due to the reason that the input is a continuous signal and output is distinct. Another certainty to conclude that the 2N quantization levels commensurate to the digital output codes Zero to Seven. Hence, the highest output of the analog to digital converter is 111 (2N - 1), corresponding to the value for which Vin/Vref >7/8. The error caused by the quantization is given in Fig. 4(b).

The value of 1 LSB for any A/D Converter can be evaluated using Eq. 2 and is given by,

1LSB= $V_{REF}/2N$ …….. eq.2

Hence for a 3-bit ADC 1LSB= $V_{REF}/8$ and

Let V_{REF} =5v then value of 1LSB equals to 0.625.

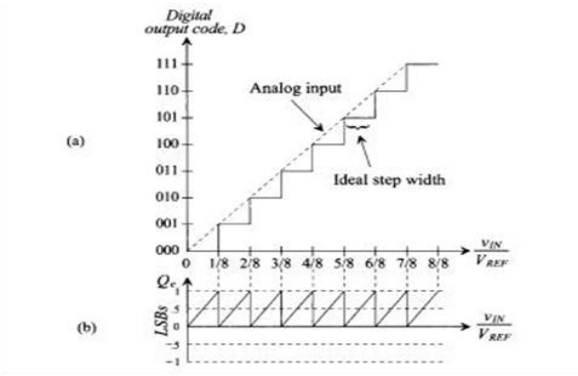


Fig-4. (a): ideal ADC transfer characteristic and **(b)** Quantization error.

The characters of the ADC are as follows:-

a) Quantization Error: - As a result of the quantization an error will be produced meanwhile the output is a discrete value and the analog input is an infinite value amount. The error, referred to as quantization error, q_e, can be precisely described as the variation among the actual analog input and the output value is in voltage. It is determined as

$q_e = V_{IN}$ -Vstair_case ……..eq. 3

the output value(Vstaircase) can be calculated as,

Vstair_case = d.(V_{LSB})=d. V_{REF} /2N ……..eq.4

where d represents the output code which is digital in nature

1 LSB in volts is the value of VLSB, that is0.625 V. The value of q_e can be converted into units of LSBs.

b) Differential Nonlinearity: - As the name suggests, Differential nonlinearity stands for some kind of non-linearity present in a difference. It is defined in a similar manner for an A/D as to that defined for a D/A Converter. However, for the Analog to digital Converter, DNL is given as the difference between the actual code width of a non-ideal converter and the code width for the ideal case.

c) Missing Codes: - As we know DNL can be measured in either LSB or volts . Outcomes of possessing a DNL equal to -1 LSB results in missing codes. A/D Converter having a DNL equal to -1 LSB is guaranteed to have a missing code. However having DNL greater than +1LSB does not guarantee to have a code missing, though probability may occur of a missing code.

d) Integral Nonlinearity: Between the first code transition and the last code transition a straight line is sketched for digital to analog converter. INL is defined as the difference among the line which is straight having no errors present and the data converter code transition points. INL is same as for analog to digital converter as well as for digital to analog converter.

e) Offset and Gain Error: - Whenever there is a variance among the value of the first code conversion and the ideal values of 1/2 LSB's Offset error occurs. The variance in the slope of a line which characteristic and the slope(k)=1 of an ideal ADC is known Gain error or scale factor error. As we can observe from Fig. 5 (a), the offset error turns out to be a constant value. We can observe from the figure that the quantization error reaches ideal stage once the initial offset voltage is resolved.

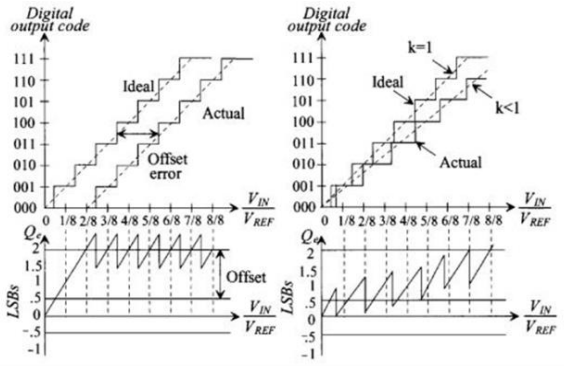


Fig-5: A/D curves for (a) offset error and (b) gain error.

f) Input Signal Bandwidth: - The bandwidth of an input signal is defined as the frequency range over which it can pass through the initial analog part of a circuit with minimum loss of amplitude. For any sinusoidal signal, it is taken as the frequency at which the amplitude drops down by 70.7 % of original amplitude.

g) Resolution: -The smallest detectable amplitude change in the input signal that can be resolved by an ADC is called its resolution. It can be calculated in terms of full scale voltage of input, but is generally represented as the number of bits used to represent the output digital signal.

h) Sample Rate: - Sampling is the basic stage for the conversion of analog signals to digital signals. The number of input samples taken per second is defined as sample rate or sampling frequency. Nyquist criteria says that to have an effective sampling and proper reconstruction of signal, if we have a maximum frequency as Fm then the sampling frequency (Fs) must be at least equal to or greater than that of twice of Fm frequency.

5. WORKING PRINCILPE OF ALGORITHMIC ADC

There are a lot of ADC's architectures available for converting analog to digital signals and each configuration has its advantages over the other. Algorithmic converters are one of them, offering [6] all the pro's of the successive approximation architecture and providing flexibility for choosing current as the information carrying quantity.

To make a pipelined algorithmic converter, we need a repeated algorithmic converter block and inserting a current-mode sample and hold blocks (SI) in between each block [7] ,hence accounting for another advantage of algorithmic ADC.

The basic concept behind the algorithmic ADC is that it samples the current signal from its previous stage(for stage I it is the input analog current signal), generates an analog residue current for the next stage, hence adding up to the reference current, compares it and produces a digital output bit. It's working principle is same as that of the pipelined structure, only difference being in pipelined the residue signal is propagated to the next stage while in this the residue is fed back to the same stage. It is a promising structure among the entire existing one's which ensures a low voltage low power applications employing current-mode [8] circuit techniques, hence acquiring low area and low power. [9]

Salama and Nairn and has proposed a small area and low power 6-bit current-mode algorithmic ADC [10] for the first time in literature, but then there's always a scope for further reducing these parameters for enhancing the performance of device and keeping it in pace with the decreasing technology node.

Keeping in mind the above constraints of low power and area [11] we have chosen to design a current-mode algorithmic ADC and the architecture is designed in accordance with the algorithm given in [12].

After so many architecture implementations in the past literature it is observed that current mode circuits are used for low power low frequency [13] ADCs with ultra-low power dissipation. [14] The basic algorithm used in this ADC is given as below and applies to every stage in a serial

manner, i.e. only after once the previous stage generates a output bit then it gets transferred to next stage and the process goes on, hence the name serial mode ADC.

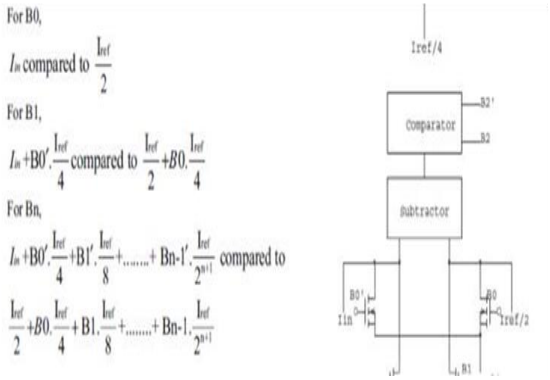


Fig-5.1: Proposed Current mode Algorithmic A/C Block Diagram

The topology for implementing the above algorithm goes as follows:

a) Stage-1 Implements a simple TIQ based reference generating current comparator, whose output is the first bit obtained as B0.

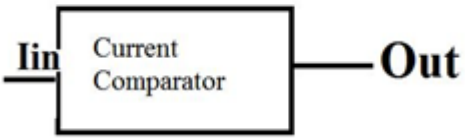


Fig-6: Stage-I of the proposed algorithmic ADC

b) Stage-II Implements a current comparator along with the digital output blocks and a 2X1 Mux, which is responsible for selecting a proper value of last bit and transferring it to the next stage.

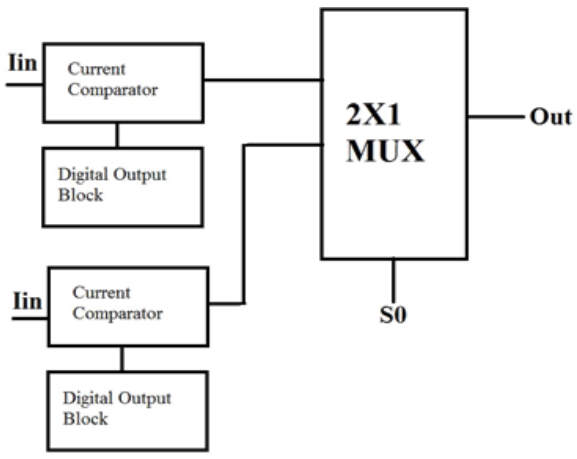


Fig-7: Stage-II of the proposed algorithmic ADC

c) Stage-III further gets complicated with a 4X1 Mux which is responsible for selecting a proper value of last two bits and transferring it to the next stage.

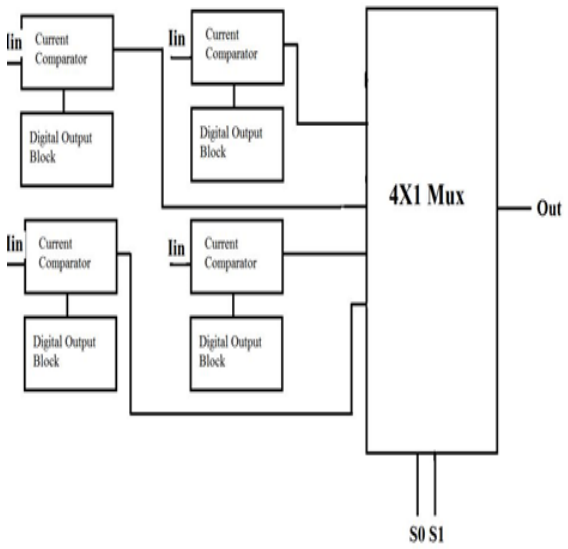


Fig-8: Stage-III of the proposed algorithmic ADC

d) Stage-IV The last stage of ADC implementing a series of blocks, wherein digital output block is responsible for adding up to the current values.

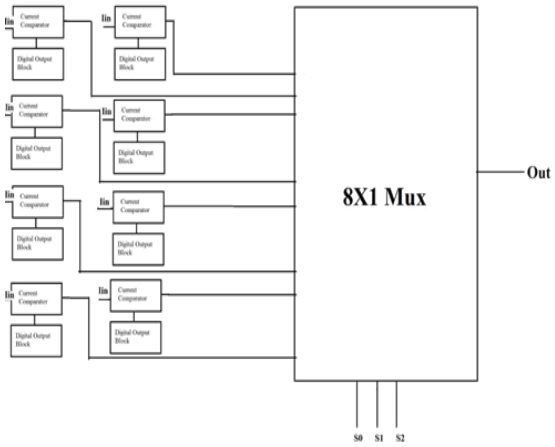


Fig-9:Block Diagram of the Algorithmic ADC

This structure produces a residue current in every stage and adds up to the next stage in the form of reference current, hence reference current of each stage differs from each other. [7]

This work of producing residue current is done by the digital block, where we have implemented transistors working with minimum sizes. [13]

6. SIMULATION RESULTS OF ADC

6.1 ADC At Lower Currents

All the block diagrams shown above are clubbed together to form an ADC as shown in Fig.9 and the ADC has

been designed for a reference current of 32uA and Input current varying from 0 to 32uA. [16]

The input current has been given in the form of a ramp signal and the corresponding output bits are obtained as shown below:

a) Ramp Input Plot

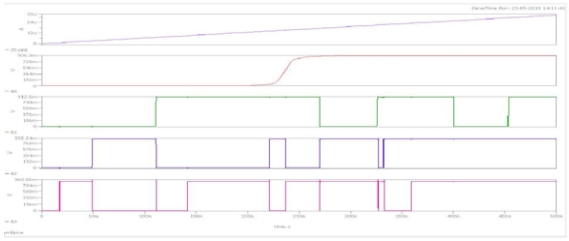


Fig-10: Output response for given ramp Input

The input current to the circuit has been given through current mirrors since it is a necessity for making a good match between transistors to preserve linearity. The reference current residue is provided by the digital block which we have implemented through current sources.

b) Digital code vs Input Current

Below graph shows an ideal behavior for the given Algorithmic ADC.

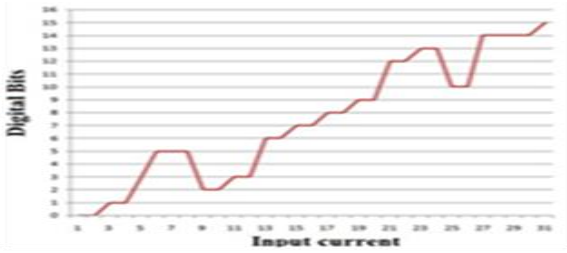
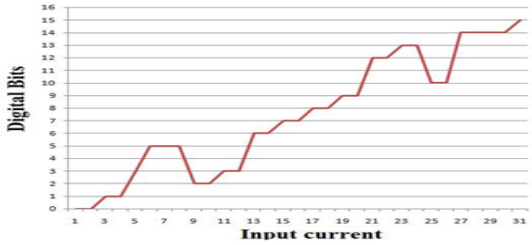
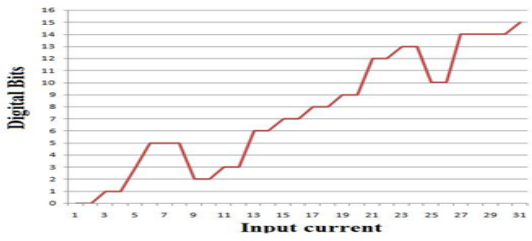


Fig-11: Bit Plot

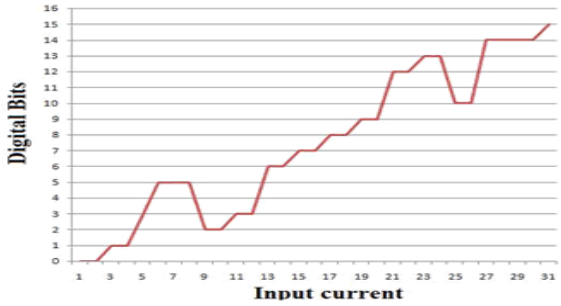
Offset error graph is shown as below:



DNL graph is given below:



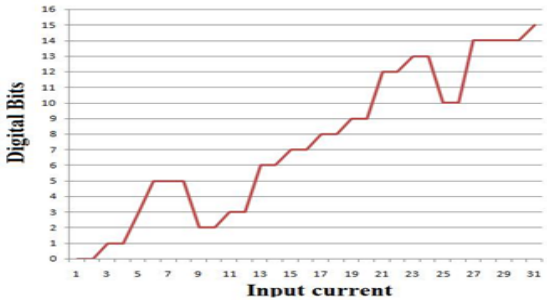
INL graph is given below:



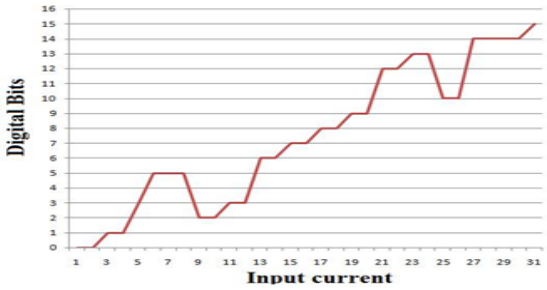
6.2 ADC At Higher Currents

All the block diagrams shown above are clubbed together to form an ADC as shown in Fig.9 and the ADC has been designed for a reference current of 32mA and Input current varying from 0 to 32mA. [17]

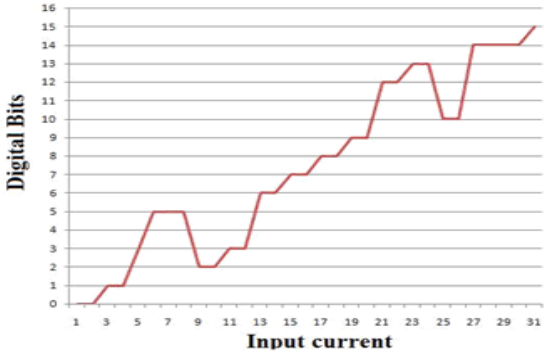
The input current has been given in the form of a ramp signal and the corresponding output bits are obtained as shown below



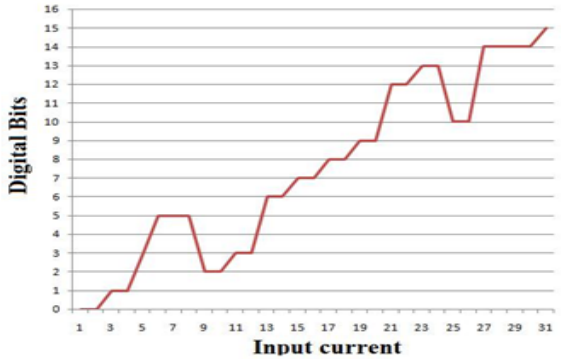
Offset error graph is shown as below:



DNL graph is given below:



INL graph is given below:



7. CONCLUSIONS

The current mode ADC is more precise and accurate than that of voltage mode ADC. As, the outputs for both lower current values and higher current values are more accurate than that of voltages and the other calculations can be done more easily with the use of current mode analog to digital converters.

In this paper we have shown the basics of ADC with their different characters, their working principle, types of ADC. Then for applying the current mode ADC we have to use some algorithms. There are several algorithms which are also included in this paper but the most precise algorithm for the implementation of current mode ADC is algorithmic ADC. Thus, for current mode ADC algorithmic ADC is used and the accurate result and precise result we get as their output. Simulation results for ADC with lower values of current and higher values of current are also shown.

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